LOW POWER FULL ADDER DESIGNS: A REVIEW

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***Abstract*— In recent years, low-power design of VLSI circuits has been identified as an essential technological need due to the high demand for portable equipments. Full adders are the most important fundamental building block in various applications such as DSP architectures and Microprocessors. This paper discusses various existing Full adder designs, consisting of different number of transistor count from one another depending on the logic styles used for their implementation. This paper focuses on the study of these designs and their comparison on the basis of performance parameters that are power consumption, delay and power delay product (PDP). The Hybrid full adder employing both Complementary CMOS and transmission gate (FA_CMOS-TG) is found to have better performance in terms of power consumption, delay and PDP in comparison to the other existing full adders. The simulation was performed using Cadence Virtuoso tools in 180nm and 90nm technology.**

Keywords—full adder; logic style; Hybrid design; low power.

I. INTRODUCTION

With the explosive growth of battery operated portable devices like laptops, cellular phones, personal digital assistants (PDAs) and notebooks, the demand for low power very large scale integration (VLSI) and ultra large scale integration (ULSI) systems have highly emerged. These devices not only require low power consumption but also high speed requirements. In various VLSI applications such as Digital Signal Processing (DSP) architectures, video and image processing and microprocessors, arithmetic operations are widely used. Addition is a fundamental arithmetic operation and is the base of many other commonly used arithmetic operation such as subtraction, multiplication, division and multiply and accumulate (MAC) in most of these systems. The 1-bit Full Adder is the fundamental building block of an arithmetic unit of systems such as adders and multipliers. Thus the performance of Full Adder directly affects the performance of the whole system. As a result, design of low-power high-speed adder has become one of the most important and essential research [1].

In order to implement 1-bit Full adder cells different logic styles each having its merits and bottlenecks have been investigated. The logic designs can be classified into two categories: 1) Static style and 2) Dynamic style. Static full adders are generally simpler with less power requirement, reliable but on chip area requirement are usually larger as compared to dynamic full adder [2] [3]. Different logic styles are liable to favor one performance aspect at the expense of the others. The logic styles used in the logic gates basically effect the speed, power dissipation, size and wiring complexity of a circuit.

This paper discusses various logic designs to implement the Full Adder. Some of the adders use one logic style while the others may use more than one logic style for their implementation. The main aim is to reduce the power and delay factors and hence decrease power-delay product (PDP) in comparison to previous ones. In this paper a brief description of Full adder using different logic style is presented.

This paper is organized as follows: section 1 describes the effect of the logic styles, section 3 describes the different logic styles to implement Full adder designs, section 4 discusses the comparison of cells on the basis of various parameters, and section 5 describes the conclusion and future work.

II. EFFECT OF LOGIC STYLES

The logic styles used to implement the logic gates basically have an impact on the speed, size, power dissipation, and the wiring complexity of a circuit. The delay in the circuit is determined by the number of inversion levels, intra- and inter-cell wiring capacitances, the number of transistors in series, and transistor sizes (i.e., channel widths). Circuit size depends on the number of transistors and their sizes (channel width) and on the wiring complexity of a circuit. Power dissipation is determined by the switching activity and the node capacitances (i.e., gate, diffusion, and wiring capacitances). The node capacitances are a function of the same parameters that also control the circuit size. Finally, the wiring complexity of the circuit is determined by the number of connections and their lengths and by whether single-rail or dual-rail logic is used. All these characteristics may vary significantly from one logic style to another and thus make the better choice of logic style important for circuit performance. The important aspects influenced by the implemented logic style are Robustness with respect to voltage and transistor scaling as well as varying process and working conditions, and compatibility with surrounding circuitries.

III. DIFFERENT LOGIC STYLES

A. Complementary CMOS full adder

Fig 1. shows the circuit diagram of complementary CMOS full adder [4]. The C-CMOS design is based on a regular CMOS structure with conventional pMOS pull-up and nMOS pull-down transistors and consists of 28 transistors. The input capacitance of a static CMOS gate is high as each input is connected to the gate of atleast an nMOS and a pMOS transistor. The series transistors in the output stage form a weak driver. Therefore, additional buffers at the last stage are required to provide the necessary driving power to the cascaded cells. The advantage of the complementary CMOS style is its robustness against voltage scaling and transistor sizing which are important to perform reliable operation at low voltages and random transistor sizes.

B. Complementary Pass Transistor Logic

Fig 2. shows the circuit of complementary pass transistor logic (CPL) [5]. The complementary pass transistor logic (CPL) uses 32 transistors in its design with swing restoration.CPL generates many intermediate nodes and their complement to make the outputs. The basic difference between the complementary CMOS full adder and complementary pass transistor logic is that the source side of the pass logic transistor network is connected to some input signals instead of power lines. In complementary PTL, the advantage is that one pass transistor network is enough to implement the logic function. Therefore, smaller number of transistors and smaller input load are required to generate the results. Pass transistor logic has an intrinsic problem that is inherent threshold voltage drop. Due to the high switching activity of intermediate nodes, high transistor count, static inverters and overloading of the inputs CPL is not an appropriate choice for low power.

C. Transmission gate adder

Fig 3. shows the circuit of Transmission gate adder (TGA) [6]. The design is based on transmission gates consisting of 20 transistors. Transmission gate consists both pMOS and nMOS transistors connected in parallel, which is a particular type of pass-transistor logic circuit. There is no voltage drop problem in transmission gate adder but it requires double the number of transistors in order to design a similar function. TGA is good for designing XOR or XNOR gates and is inherently low power consuming. The main disadvantage of this logic style is that it lacks driving capability. When TGA are cascaded their performance degrades significantly.

D. Transmission function full adder

Fig 4. shows the circuit of Transmission function full adder (TFA) [7]. A transmission function full adder is based on transmission function theory. This adder consists of 16 transistors, for the realization of the circuit. The transmission full adder uses both pMOS and nMOS transistors for its implementation. It requires fewer MOS transistors in comparison with the previous one.There are two possible short circuit paths to the ground. There is no voltage drop problem. Transmission functional adder (TFA) is inherently low power consuming same as Transmission gate adder (TGA). TFA is also good for designing XOR or XNOR gates. The disadvantage of these logic styles (i.e., TGA and TFA) is that they lack driving capability. When TFA are cascaded, their performance degrades significantly and hence degrading the performance of the system in terms of power, delay and area.

E. 14T full adder

Fig 5. shows the circuit of 14T full adder [8]. 14T full adder uses more than one logic style for its implementation and is a Hybrid logic design style. 14T full adder utilizes the low power XOR/XNOR circuit and a pass transistor network. They generate a non full swing sum signal and also uses four transistors to generate a full swing carry signal. 14T full adder lacks driving capability and their performance degrades drastically when cascaded.

F. 10T full adder

Fig 6. shows the circuit of 10T full adder [9]. 10T full adder also uses more than one logic style for its implementation and is a Hybrid logic design. In order to implement the addition logic function the design of the 10T full adder cell are based on an optimized design for the XOR function and pass transistor logic. Two XOR operations generate the sum signal, each XOR operation requiring 4T transistors. 10T full adder also lacks the driving capability and their performance degrades drastically when cascaded same as that of 14T.

G. HPSC full adder

Fig 7. shows the circuit of HPSC (Hybrid pass logic with static CMOS) full adder [10]. Hybrid pass logic with with static CMOS output drive full adder was proposed by Zhang et al. In the implementation of HPSC adder XOR/XNOR functions were simultaneously generated by pass transistor logic by using only 6T transistors. These XOR/XNOR signals were given as input to the CMOS module to generate the full swing output s of the full adder. The disadvantage of HPSC

full adder was the increased transistor count and decreased speed.

H. 24T full adder

Fig 8. shows the circuit of 24T full adder [11]. The 24T full adder is composed of pass transistor logic and static CMOS logic. The sum output is generated by the pass transistor logic module and needs 12T transistors while as the mirror type static CMOS logic generates the carry output and also requires 12T transistors. Therefore, the total transistor count of the this full adder is 24. The disadvantage of this 24T full adder is that the transistor count is very high and degrading the performance parameters like power and delay.

I. Low-power high-speed Hybrid full adder (16T)

Fig 9. shows the circuit of 1-bit Hybrid full adder [12]. This adder employs both (CMOS) logic and transmission gate logic. This hybrid full adder consists of 16T transistors. The XNOR modules generate the sum output. The carry output is generated through transmission gates. The XNOR modules are responsible for reduction in power consumption by deliberate use of weak inverters (channel width of transistor is small). Also the carry generation module is responsible for reducing the overall propagation delay by the use of strong transmission gate (channel width of transistor is large). Hence, overall performance of the system is improved.

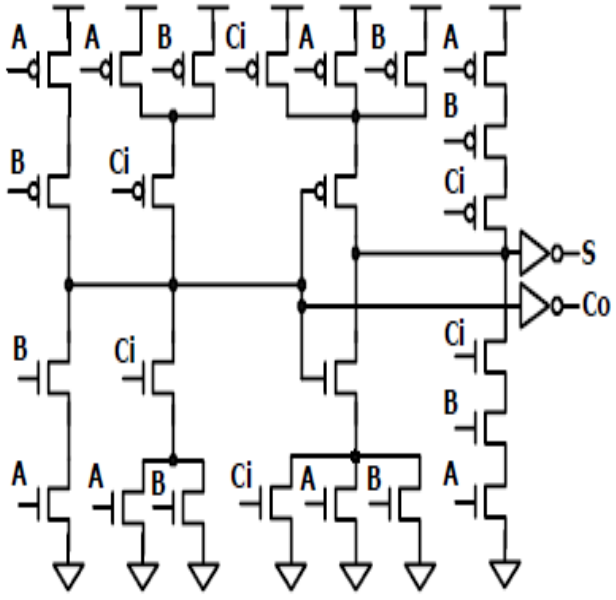

Fig 1. Conventional CMOS Full Adder

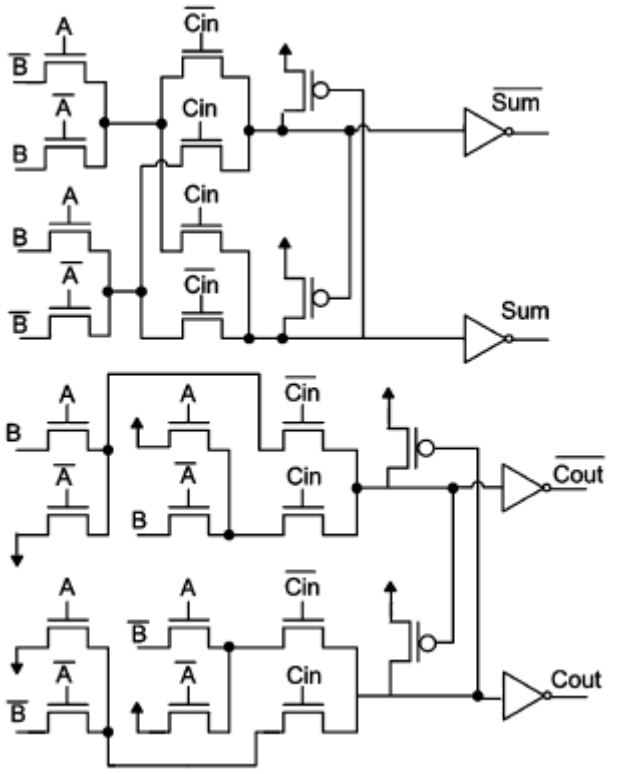

Fig 2. Complementary Pass Transistor Logic

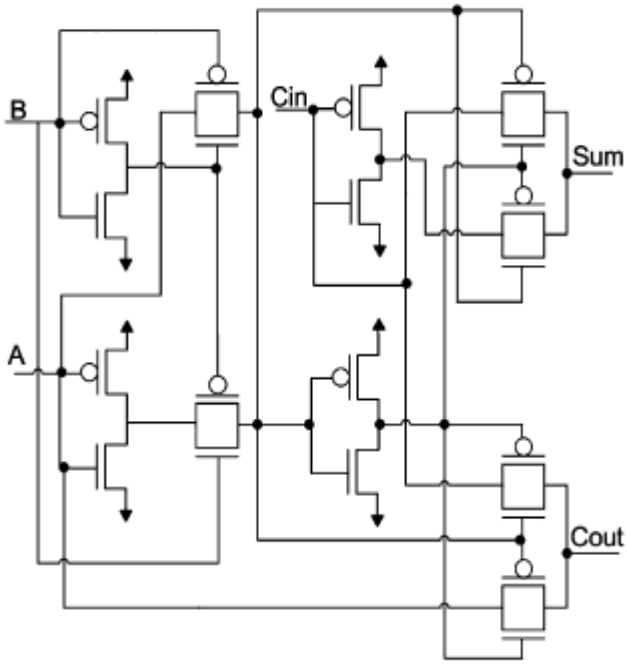

Fig 3. Transmission Gate Adder

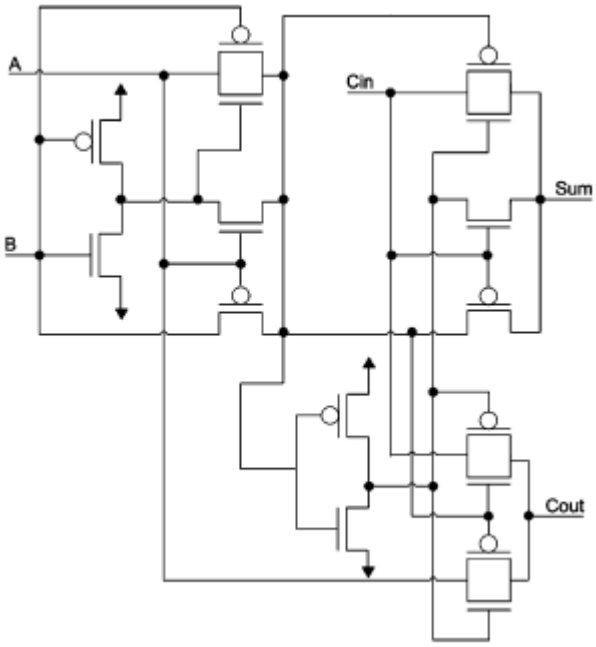

Fig 4. Transmission Function Adder

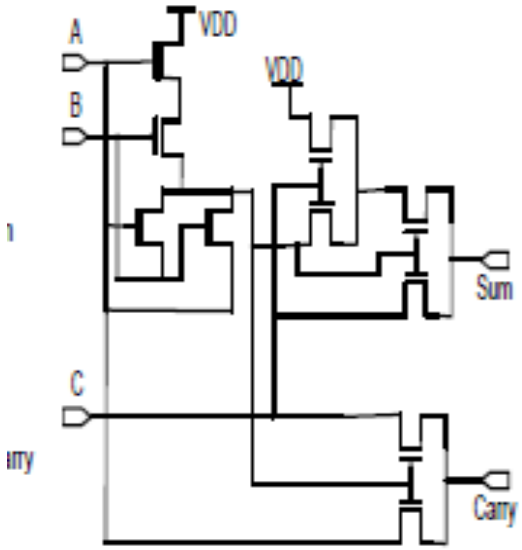

Fig 6. 10T Full Adder

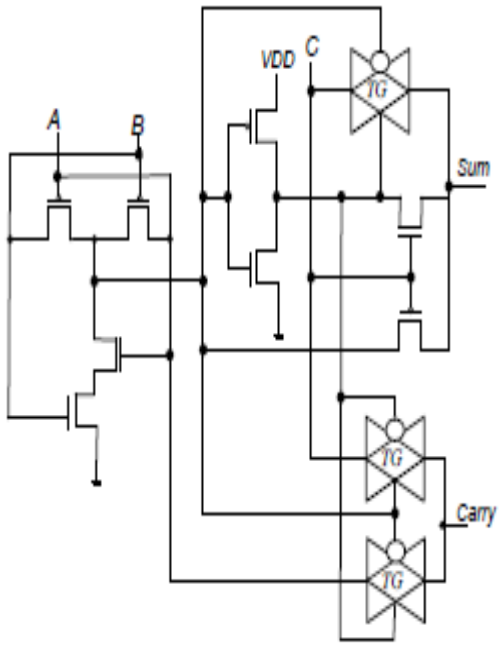

Fig 5. 14T Full Adder

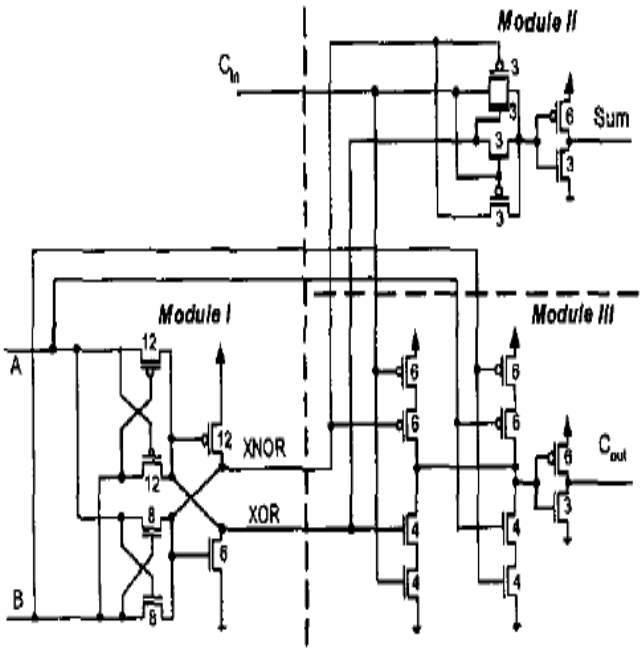

Fig 6. HPSC adder

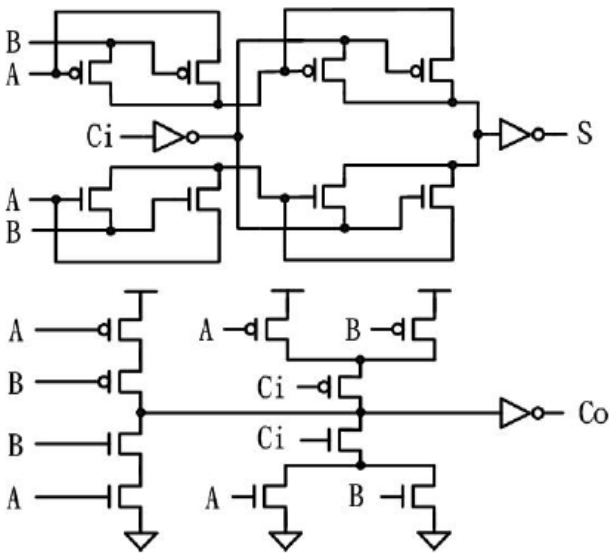

Fig 7. 24T adder

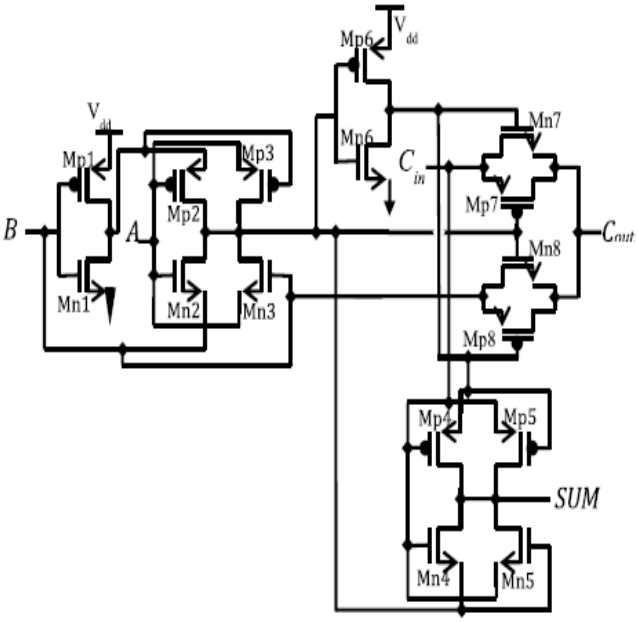

Fig 8. Low-Power High-Speed Hybrid Full Adder

IV. COMPARISONS OF THE RESULTS

In this section all the discussed Full adders are being compared on the basis of power consumption, delay, and power delay product (PDP). These simulations are being done in 180nm and 90nm environment by using Cadence Virtuoso tools. Table 1 and Table 2 shows the comparison of different Full adders on the basis of performance parameters that are power consumption, delay and PDP [12].

Table 1. Comparison results for Full adder in 180nm technology.

Design	Average Power (µw)	Delay (ps)	PDP (fJ)	Transistor Count	References
C-CMOS	6.2199	292.1	1.816832	28	[4]
CPL	7.71985	183.97	1.42022	28	[5]
TFA	8.2491	287.1	2.368316	16	[6]
TGA	8.4719	293.9	2.8989	20	[7]
14T	12.7217	381.7	4.85587	14	[8]
10T	14.3449	132.595	1.902062	10	[9]
HPSC	6.3798	273.7	1.74615	22	[10]
24T	15.91	314.2	4.998	24	[11]
FA_CMOS-TG	4.1563	224	0.931	16	[12]

Table 2. . Comparison results for Full adder in 90nm technology.

Design	Average Power (µw)	Delay (ps)	PDP (fJ)	Transistor Count	References
C-CMOS	1.5799	0.1269	0.200489	28	[4]
CPL	1.7598	0.0791	0.1392	28	[5]
TFA	1.7363	0.3198	0.55526	16	[6]
TGA	1.7619	0.2317	0.40823	20	[7]
14T	3.3297	0.3389	1.12843	14	[8]
10T	----	----	----	10	[9]
HPSC	1.56	0.2207	0.34429	22	[10]
24T	7.707	0.1406	1.0836	24	[11]
FA_CMOS-TG	1.17664	0.0913	0.107427	16	[12]

V. CONCLUSION AND FUTURE WORK

In this paper different full adders implemented using single or the hybrid logic styles have been compared on the basis of different performance parameters that include power

consumption, delay and PDP. The simulation results show that the 1-bit hybrid full adder (FA_CMOS-TG) has the improved performance parameters than the other logic designs. Thus, FA_CMOS-TG has reduced power consumption, delay and PDP that improves the performance of the whole system.

In future, these performance parameters can be further improved by implementing the full adder using a new hybrid logic style. The hybrid of PTL and GDI technique can be used to obtain the better results. After the text edit has been completed, the paper is ready for the template. Duplicate the template file by using the Save

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