Analysis of New 7- Level an Asymmetrical Multilevel Inverter Topology with Reduced Switching Devices

Nikhil Agrawal, Praveen Bansal

Abstract— **Inverter is a power electronics device that converts DC power to AC power at desired voltage and frequency. In the last few years the application of multilevel inverter increase as it has capability to handle high power and voltage with lower harmonic distortion. As level of inverter increases the harmonic content in the output voltage decrease and at the load end good quality of power available which makes operation efficiently.**

In this paper 7- Level an asymmetrical multilevel inverter topology proposed with using H-bridge and with other switches and voltage sources to analyses the performance of MLI in terms of total harmonic distortion and power components.

This paper work on 7- level multilevel inverter structure with level shifted pulse width modulation (PWM) technique. The pulse width modulation techniques used to improve the output results.The aim of this proposed topology to reduce the circuit complexity as less use of switches and total harmonic distortion and improved the quality of power and efficiency. The results of proposed 7-Level Asymmetrical multilevel Inverter are shown using MATLAB/SIMULINK software.

Index Terms— **H- bridge multilevel inverter, Total harmonic Distortion (THD), Pulse width modulation (PWM), Asymmetrical multilevel inverter (ASMLI).**

1) INTRODUCTION

Multilevel inverter is the power electronic converters that are widely used in power industry applications. In the recent years, multilevel inverter have more attention and importance in the power industry because of their high frequency and high voltage operation capability, low electromagnetic interference (EMI) and high efficiency[1].

Multilevel is inverted during the 1975 [2]. The necessity of multilevel inverter, as the level of inverter increases the output voltage waveform tends to near the sinusoidal waveform that means the harmonic content in the output voltage waveform decreases and the quality of power at load end is good that improve the operation and reliability of load equipment [7].

Multilevel inverter in comparison with conventional two level inverters, have lower harmonic components, lower switching losses, high power quality output, high efficiency and reliability and low dv/dt stresses [3].

In multilevel inverter, to produce high level of voltage, the components increase that make circuit complex and expensive that is the disadvantage of multilevel inverter over the two level inverter.

The conventional multilevel inverter topologies like flying capacitor multilevel inverter (FCMLI), diode clamped or neutral point clamped multilevel inverter (NPCMLI)[3] and Cascade H- bridge multilevel inverter (CHBMLI)[4] when used for large number of voltage level , the device count increased in large number that makes complexity in implementation and high cost due to this drawback a new topology being proposed that reduce the devices for large voltage level in comparison to conventional topologies. The multilevel inverter also classified in two types as Symmetrical Multilevel inverter and Asymmetrical Multilevel inverter. The asymmetrical structure uses different magnitude of voltages that help in produce high voltage level with reduced devices in comparison to symmetrical structure [5-6].

The innovations in topological structure are being integrated with suitably selected modulation scheme and control strategies to minimize the requirement of switching devices.

In this paper, a new multilevel inverter topology proposed [8] with asymmetrical structure with a simple structure. The structure such that it can synthesize all the additive and subtractive combination of the input DC levels. In this paper the analysis of 7- Level asymmetrical multilevel inverter is presented and simulation result and total harmonic distortion results are shown in the section 5.

2) PROPOSED TOPOLOGY

The proposed topology structure for 7-Level asymmetrical multilevel inverter are shown in the fig 1. The proposed topology have simple configuration with eight switches and two voltage sources. The magnitude of voltage sources are V and 2V. The main purpose of this proposed ASMLI topology is to control the EMI, minimize the total harmonic distortion with different PWM techniques and it also minimizes switching device than conventional multilevel inverter. For a conventional single-phase 7-level inverter, it Uses 15 devices for CHBMLI, 49 switches for NPCMLI and 34 devices for FCMLI whereas the proposed topology uses only 10 devices.

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As in table 1 shows the switching scheme of proposed topology, as switches S3, S4, S6, S8 are Turned ON the output voltage will be +3Vdc. And the switches S2, S4, S6, S8 are turn ON the +2Vdc output voltage obtain i.e. +2 Level voltage and so on.

The proposed topology inverter uses power devices as Metal-oxide semiconductor field- effect transistor (MOSFET) and Insulated gate bipolar transistor (IGBT) is depend on the selection of magnitudes of voltage sources.

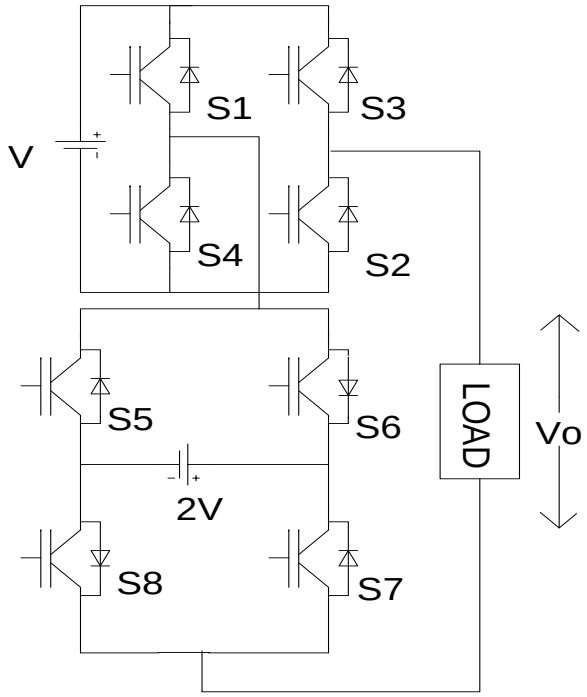


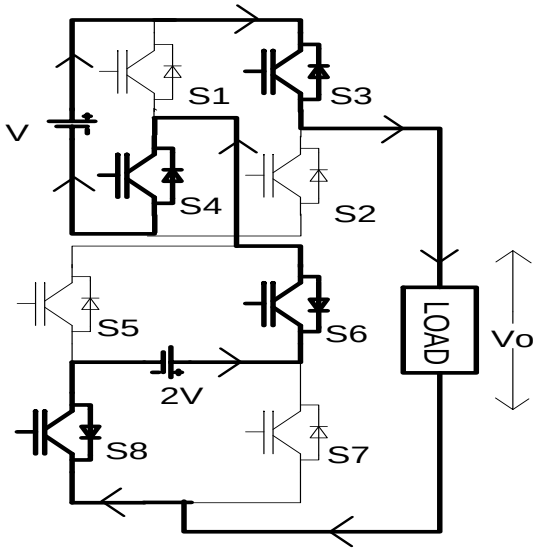
Fig 1. Proposed Topology 7- Level Asymmetric MLI

In the proposed topology the analysis is done to resistive load the simulation results are shown in section 5 for resistive load.

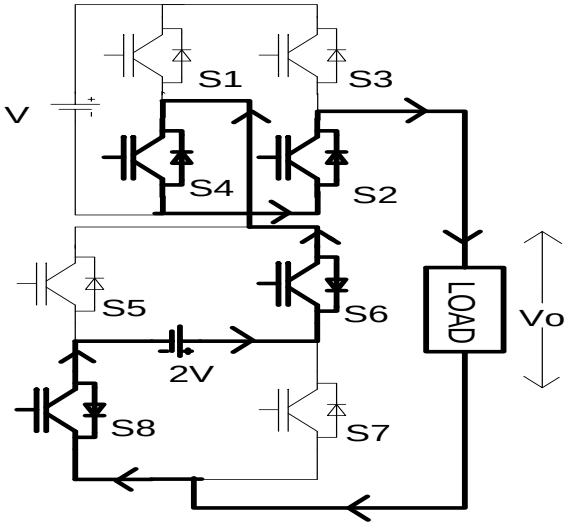
TABLE 1: SWITCHING SCHEME OF PROPOSED 7- LEVEL ASYMMETRICAL MLI

OUTPUT VOLTAGE	S1	S2	S3	S4	S5	S6	S7	S8
+3 V	OFF	OFF	ON	ON	OFF	ON	OFF	ON
+2 V	OFF	ON	OFF	ON	OFF	ON	OFF	ON
+1 V	OFF	OFF	ON	ON	ON	OFF	OFF	ON
0 V	OFF	ON	OFF	ON	ON	OFF	OFF	ON
-1 V	OFF	OFF	ON	ON	OFF	ON	OFF	ON
-2 V	OFF	OFF	ON	ON	OFF	ON	ON	OFF
-3 V	OFF	ON	OFF	ON	OFF	ON	ON	OFF

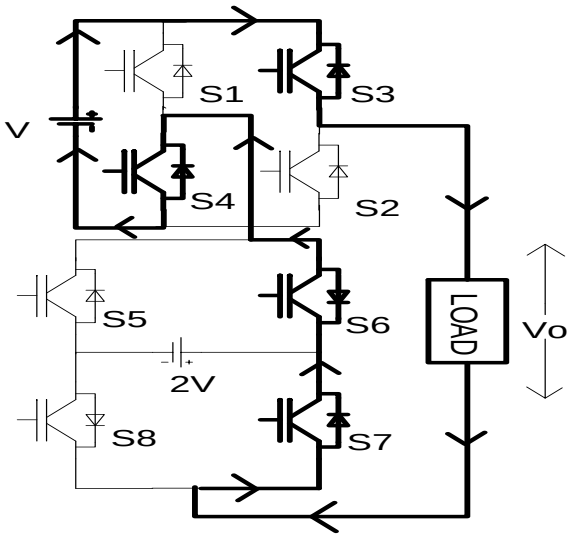
3) OPERATING MODES



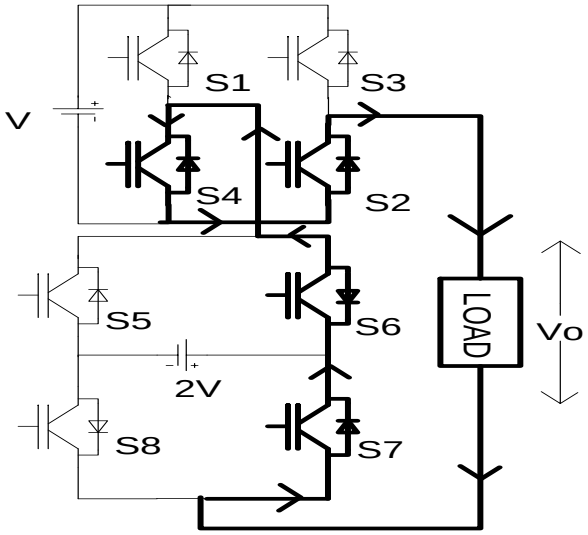
Level +3 v
Fig. (a)



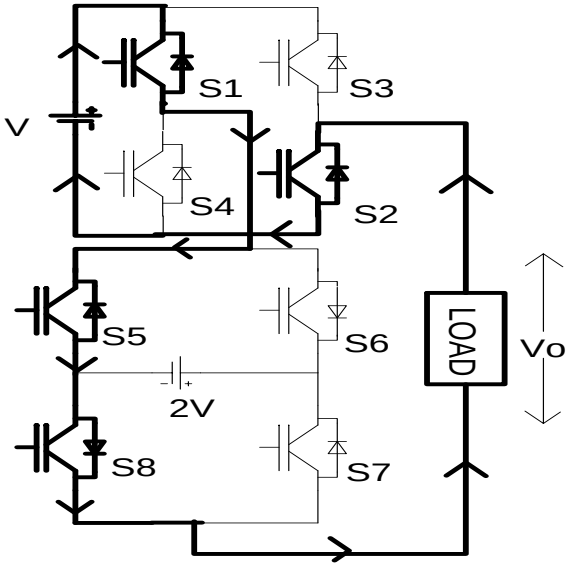
Level+2 V
Fig. (b)



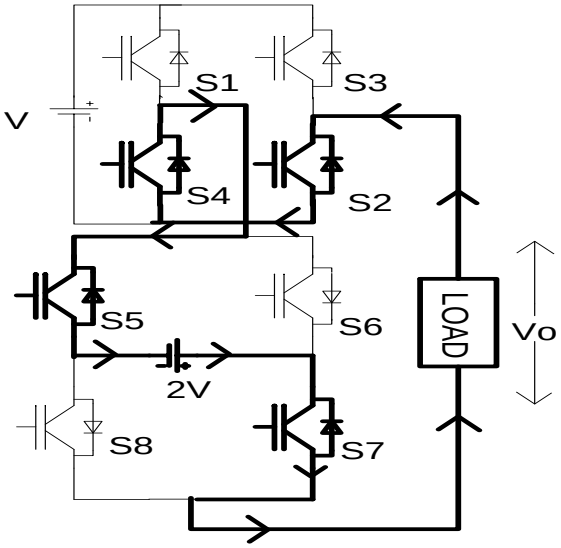
Level +1 V
Fig. (c)



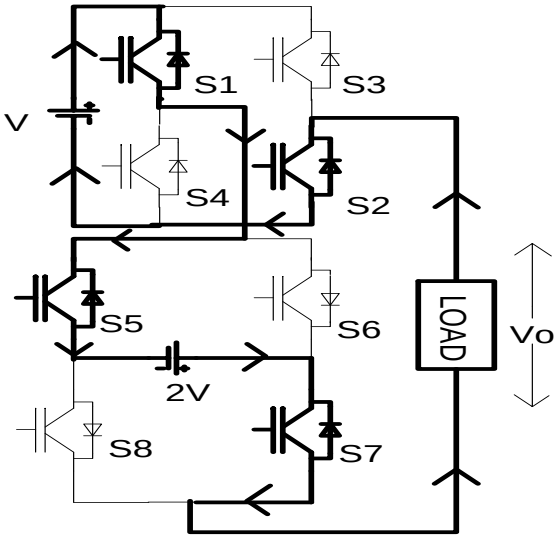
Level 0 V
Fig. (d)



Level -1 V
Fig. (e)



Level -2 V
Fig. (f)



Level -3 V
Fig. (g)

Fig. 2 Fig. (a), Fig. (b), Fig. (c), Fig. (d), Fig. (e), Fig. (f), Fig. (g) are the operating modes of proposed Topology

The operating modes shown in fig.2 for every voltage level. In the figure the turned ON devices and operating path is shown in the darkest line and turned off device are shown in normal line. The arrow indicates the direction of path. Here load is resistive.

TABLE 2: COMPARISION OF COMPONENTS BETWEEN PROPOSED AND CONVENTIONAL TOPOLOGIES

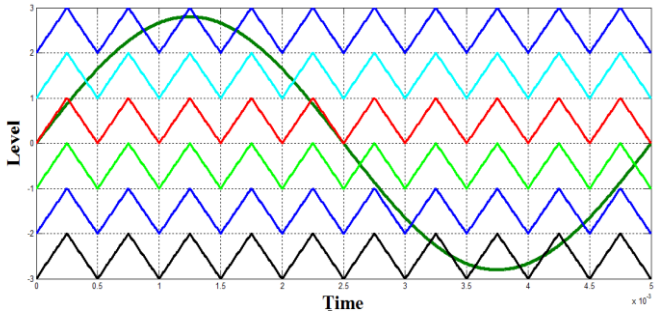
MLI STRUCTURE COMPONENTS	CASCADE H-BRIDGE	DIODE CLAMPED	FLYING CAPACITOR	PROPOSED TOPOLOGY
MAIN SWITCH	12	12	12	8
CLAMPING DIODES	–	30	–	–
DC SPLIT CAPACITOR	–	6	6	–
CLAMPING CAPACITOR	–	–	15	–
DC SOURCES	3	1	1	2
TOTAL	15	49	34	10

4) MODULATION STRATEGIES

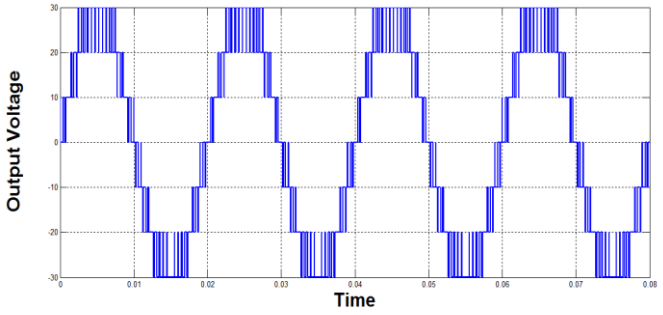
There are different Level shifted pulse width modulation (PWM) techniques [9-10] to control the output voltage.

A) Phase Disposition (PDPWM):

In Phase disposition pulse width modulation technique all carrier above and below the zero reference are in same phase.



(a)

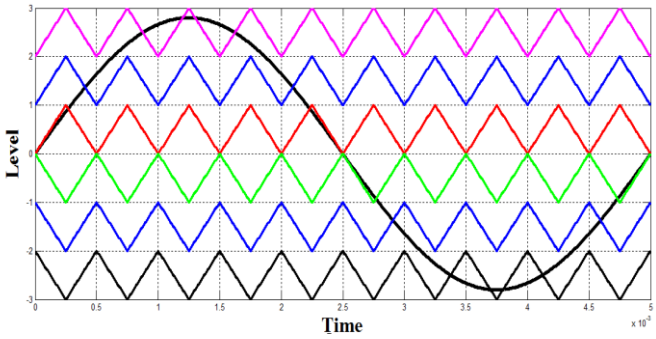


(b)

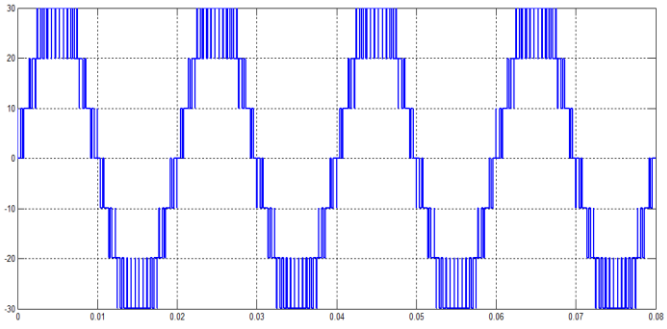
Fig 3. (a) Carrier Arrangement and (b) Output Voltage of PDPWM technique

B) Phase Opposition Disposition PWM (PODPWM):

In this modulation techniques all carrier above zero reference and below the zero reference also in same phase but 180° out of phase with above and below the zero reference.



(a)

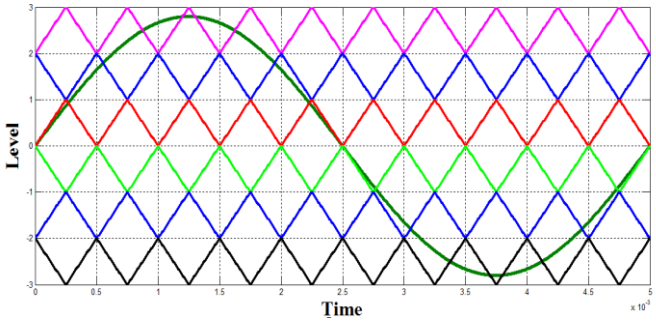


(b)

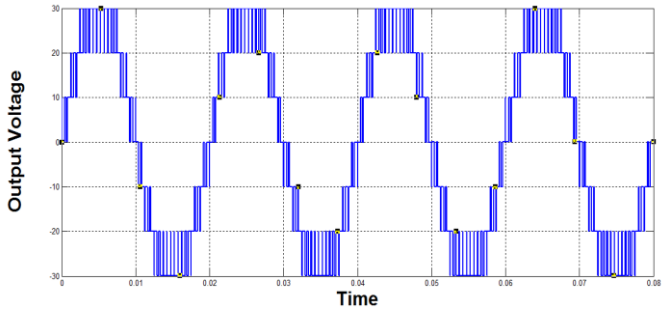
Fig 4. (a) Carrier Arrangement and (b) Output Voltage of PODPWM technique

C) Alternative Phase Opposition Disposition PWM (APODPWM):

In alternate phase opposition Disposition pulse width modulation scheme every carrier is out of phase with its neighbor carrier by 180°.



(a)



(b)

Fig 5. (a) Carrier Arrangement and (b) Output Voltage of APODPWM technique

5) SIMULATION RESULT

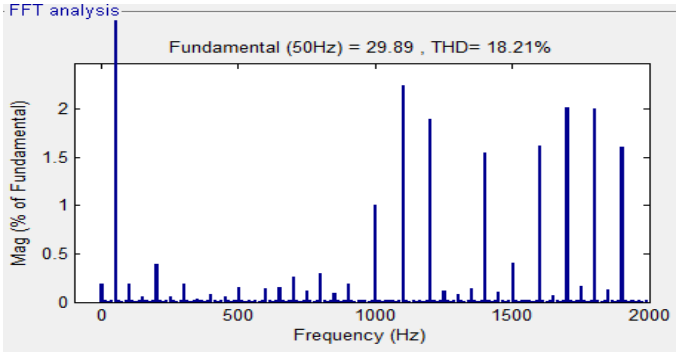


Fig 6. FFT Of 7 –Level asymmetrical MLI with PD Modulation scheme and 1.0 Modulation index

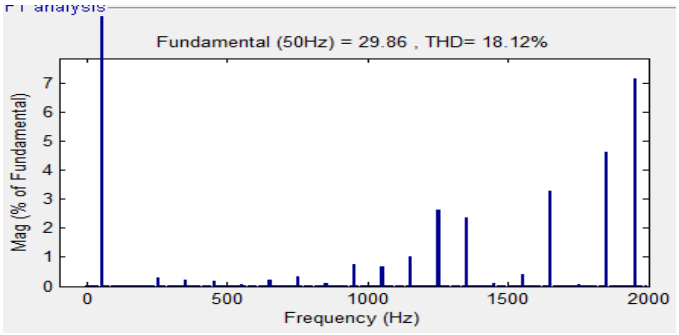


Fig 7. FFT of 7- Level asymmetric MLI with POD Modulation Scheme and 1.0 modulation index

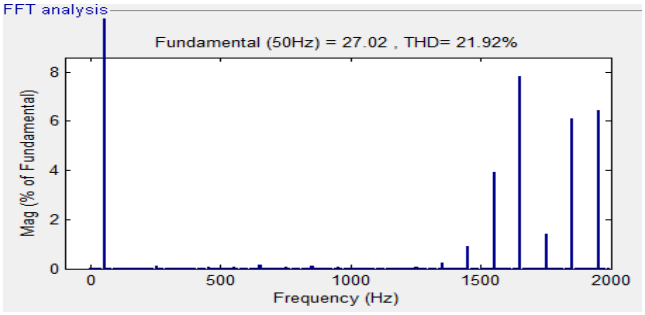


Fig 8. FFT of 7-Level asymmetric MLI with APOD Modulation Scheme and 0.9 Modulation index

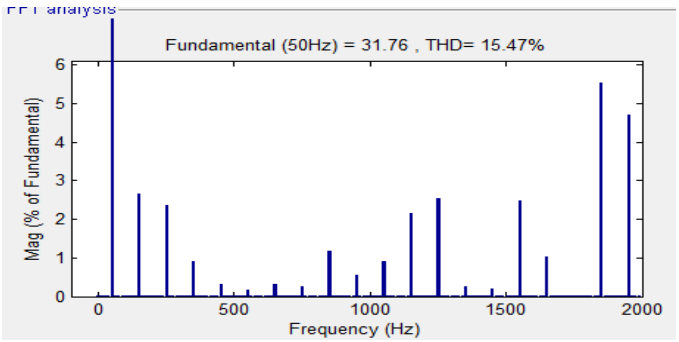


Fig 9. FFT of 7- level asymmetric MLI with POD Modulation scheme and 1.1 modulation index

TABLE 3: COMPARISION OF DIFFERENT MODULATION TECHNIQUES RESULT

Level	Modulation index	PWM Techniques		
		PD	POD	APOD
7 level	1.1	15.69	15.47	15.72
	1.0	18.21	18.12	18.34
	0.9	22.38	22.05	21.92
	0.8	24.23	24.00	24.12

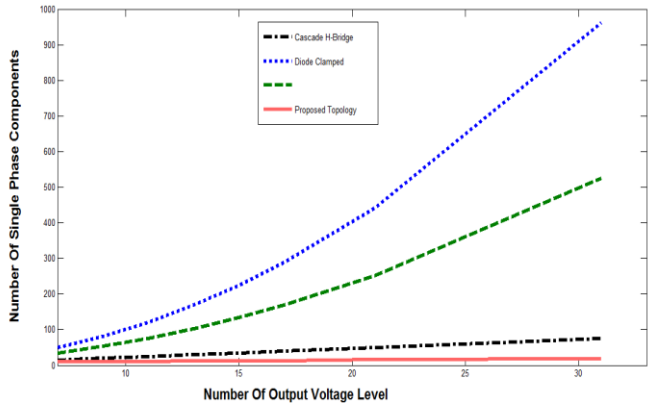


Fig 10. The graph between required single phase component for different Level of MLI topology

6) CONCLUSION

This paper conclude that the proposed topology require less number of devices as compare to conventional multilevel inverter topology as shown in the TABLE 2 and figure 10. And this paper shows the simulation result for 7- Level asymmetrical multilevel inverter with three, level- shifted pulse width modulation techniques and result of these techniques are compare in the TABLE 3. The lowest THD is obtain in PODPWM technique with 1.1 Modulation index.

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REFERENCES

[1] Rodriguez, J., Jih-Sheng, L., Fang Zheng, P. Multilevel inverters: a survey of topologies, controls, and applications", IEEE Trans. Ind .Electron. 2002, 49, pp. 724–738.
[2] R.H. Baker, "High-voltage converter circuits", U.S. patent Number 4, 203, 151, May 1980.
[3] Nabe, I. Takahashi and H. Akagi. "A new neutral point clamped PWM inverter." IEEE Trans. Ind. Applicate. Vol. 1A-17, pp 518- 523, Sep. /Oct. 1981.
[4] B. M. Song, S. Gurol, C. Y. Jeong, D. W. Yoo, and J. S. Lai, "A soft-switching high-voltage active power filter with flying capacitors for urban maglev system applications," in *Conf. Rec. IEEE-IAS Annu. Meeting*, Chicago, IL, Sept. 2001, pp. 1461–1469.
[5] Kiruthika, C., Ambika, T., Seyezhai, R.: Implementation of digital control strategy for asymmetric cascaded multilevel inverter"International Conference on Computing, Electronics and Electrical Technologies (ICCEET), 2012, pp. 295–300.
[6] S.J.V. Prakash,M. Vishnu Prasad, "comparison between symmetrical and asymmetrical single phase seven-level cascade H-Bridge Multilevel inverter with PWM topology" in international Journal of multidisciplinary sciences and engineering,vol.3No.4,April 2012.
[7] Colak, I., Kabalci, E., Bayindir, and R.: „Review of multilevel voltagesource inverter topologies and control schemes", Energy Convers. Manage, 2011, 52, (2), pp. 1114–1128.
[8] Sandira segarane , Jeevarathinam Baskaran, Subburam Ram kumar, seenithangam Jeevananthan, "Cross-Switched multilevel Inverter using Auxiliary reverse-connected voltage sources" in IET Power electronics, 2013.
[9] M. Manjrekar and G. Venkataramanan, "Advanced topologies and modulation strategies for multilevel inverters," in *Proc. IEEEPESC'96*, Baveno, Italy, June 1996, pp. 1013–1018.
[10] K. Jang-Hwan, S.-K. Sul, and P. N. Enjeti, "A carrier based PWM method with optimal switching sequence for a multilevel four-leg voltage source inverter," IEEETrans. Ind. Appl., vol. 44, no. 4, pp. 1239–1248, Jul. /Aug. 2008.

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