Low-power pulsed hybrid flip-flop based on a c-element

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ABSTRACT-This paper presents a new flip-flop design featuring implicit pulse-triggered structure which consist of a dynamic front-end stage and a static back-end, and hence, it is considered as a hybrid flip-flop seises both low-power as well as high-performance targets. Proposed flip-flop is implemented by using a sampling circuit, a C-element for rise and fall paths, and a keeper stage. Simulation is done in 45 nm CMOS technology with a 1 V supply voltage which shows that 27.8% and 16.9% reductions in form of power consumption as compared to other flip-flop designs in 25% and 50% data activities, respectively. Furthermore, by using four clocked transistors with transition condition technique make this design more fast and power-efficient in all factors, and contest 5% enhancement in speed. Therefore, other exploitable advantage of presented design is power-delay-product (PDP_{DQ}) index whose improvement ranges from 16.7% to 56%. It is also betoken that presented scheme having negative setup time near zero and significant hold time contains only 17 transistors that affecting the layout area efficiency by almost 12%.

Keywords—Flip-Flop,Low-power,C-element,Data activity, Process variation.

1. Introduction

The most important performance criteria in designing system on chips (SoCs) are to reduce area, power dissipation, and delay [1]. Flip-flop (FF) is the basic storage element and as considered as one of the major elements in VLSI design [2]. for obtaining a high performance and low power design it is important taken into account the FFs [3]. The most important factor in modern VLSI technology for all those device which are easy to define and handheld applications is low power consumption [4]. As the clock system occupies 30–60% of the die power. Clock system is the major source of power dissipation on chip power which is built of flip flop and clock distribution network [5,6].The main issue in flip flop is Power consumption and delay. So, to meet low power requirement and for reducing the delay of devices flip flop can be classified into two groups-master slave and pulsed flip-flops [5–8].

Pulsed flip-flop is used to gives the negative setup time and to meet the low area and power of the flip-flops [9]. To reduce the circuit complexity, pulse-triggered FFs have been considered as a popular alternative to the conventional master-slave-based FF these days. A pulse-triggered FF comprise of a pulse generator (also called transition detector) for strobe signals together with a latch for data storage. Since the pulses are generated on the P-FFs appear in two types: Pulse-triggered FFs (P-FFs) can be classified into two types, that is, implicit and explicit, depending on the implementation of pulse generator [10-12]. In implicit type P-FF, the pulse generator is a built-in logic of the latch design, and no explicit pulse signals are generated. In explicit type P-FF, the designs of pulse generator and the latch are separate. Even though implicit pulse generation is usually considered as more power efficient, the lengthened signal discharge path in latch design leads to inferior timing characteristics.

This paper is reviewed on a work that includes a variety of flip-flop designs to meet the area-power efficient with high performance features. The PowerPC is the flip-flop which consists of these entire features to some extent [13]. The flip-flop that provides high-performance and low-power and also offers high speed but consumes high power due to large CLK load is the semi-dynamic flip-flop [14]

Recently, a flip-flop is introduced to improve the power consumption by reducing precharge capacitance factor called as high speed dual-edge triggered modified hybrid latch flip-flop [15].

With the help of C-element, a new pulsed hybrid flip-flop is introduced in this paper where, C-element is used as a fundamental stage of its structure which overcomes the drawback of additional switching activity and provides improvement from 7.9% to 55.5%.

Whereas pulsed latches are choose for the application where targeting energy efficiency from moderate to high performance [19].

This paper is divided into the following manner- section 2 reviews the five flip-flop structure [14-18], and explain some of their disadvantages. Section 3 presents the proposed flip-

flop and its operation. Section 4 provides the simulation and finally the conclusion.

2. Literature review

To have a fair comparison of performance, some of the most advanced existing FF designs are reviewed in this paper and illus-trated in Fig. 1. Semi-dynamic flip-flop (SDFF), shown in Fig. 1(a), is a design which composed of a dynamic stage coupled to a pseudo-static one. Two groups of inverter connected back-to-back are employed in this scheme, i.e., I5, I6 inverters and I7, I8 inverters. The former group is used to latch data while the latter one is employed to hold node X. Transparent window is confined by two inverters as well as NAND function. Although this flip-flop is a well-suited choice for high-performance applications, it is not preferable for power consumption targets because of high switching activity related to its clock pulse generator as well as of the highly loaded internal node X. Notably, the challenge with SDFF is the susceptibility to the "static-one-hazard" manifesting as input and output are both high. This contributes substantial power consumption due to glitches [14,18,20,21].

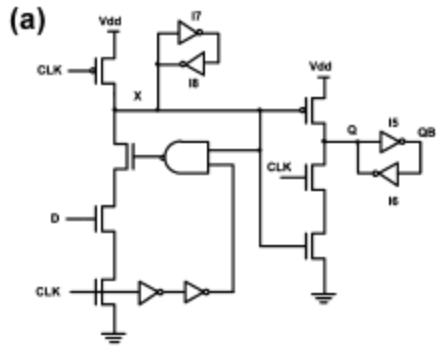
Another flip-flop which is introduced in [15] is high speed dual-edge triggered modified HLFF (HSDMHFF) is illustrated in Fig. 1(b). It is an implicit-pulsed double edge triggered flip-flop whose first stage is responsible for generating some clock delay signals which are inserted in the second stage. This design suffers from additional switching activity on dynamic node resulting in more power consumption especially in low activity factors. On the other hand, at the falling edge of CLK, it takes more time to discharge due to inverter's latency. Additionally, number of clocked transistors in this design is 12 contributing a lot of power consumption. [15,22].

Fig. 1(c) shows dynamic explicit pulsed triggered flip-Flop (DEPFF) including a pulse generator and a pulsed latch. It is a flip-flop where its pulse generator creates a brief pulse at both of clock edges. The pulse width is specified by delay of four inverters whose skew provides a wide transparent window. Including transistor N2 in the discharging path ensures that there would be no superfluous switching activity of node X once D keeps high. However, this design suffers from considerable power consumption when operating in low switching activities, mainly owning to the power overhead of the pulse generator built from many clocked transistors having activity factor of 100% [16].

Fig. 1(d) depicts a design called single-ended conditional capturing energy recovery (SCCER). This flip-flop is an implicit pulse type

Where transistor N3 is subject to the output feedback plays role of conditional capturing. On the other hand, the path enabling a fall output Q transition is statically designed and does not require conditional capturing. Pseudo NMOS logic associated with first stage tends to have low short circuit power dissipation. Data keeper that imposed some limitations on this circuit is eliminated, which translates into a low parasitic capacitance at node X. A newly employed inverter I2 assumes control of transistor N5 via connecting to its gate terminal. The pulse controlled discharging circuit is shared by rise and fall output paths. However, this design encounters draw-back of low speed due to prolonged discharging path made up four series-connected transistors [17,23].

Dual dynamic node flip-flop (DDFF) design is comprised two separate dynamic nodes driving pull down and pull up devices as shown in Fig. 1(e) where an unconditional shutoff mechanism is realized at its front end stage. Depending on the state of CLK, the functionality of DDFF can be categorized into two phases; evaluation and precharge. The former phase occurs when CLK is high, and the latter one happens as CLK is low. The actual data latching operation allowing D to propagate to Q occurs during interval that confined by the 1–1 overlap of CLK and CLKB. When D is high before this overlap period, node X1 is pulled down through NM0-2, which changes the state of inverter pair INV1-2, resulting in node X1B pulling up and node QB making a fall transition through NM4. Inverter pair INV1-2 make node X1 hold high voltage level. Hence, as long as evaluation interval continues, node X2 is maintained high. When CLK goes low, precharge phase begins in which node QB is kept stable at its previous value. Subsequently, in case D is low before overlap period, pull down path is disconnected, and node X1 experiences the rise transition through PM0. Afterwards, node X1B assumes zero voltage level. As soon CLK goes high, NM3 is on, X2 is discharged to zero, and node QB is pulled up through PM2 [18].



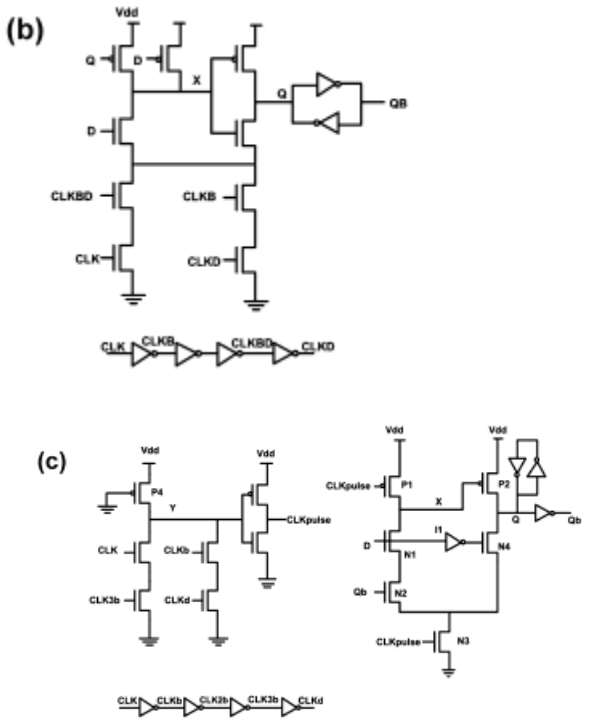
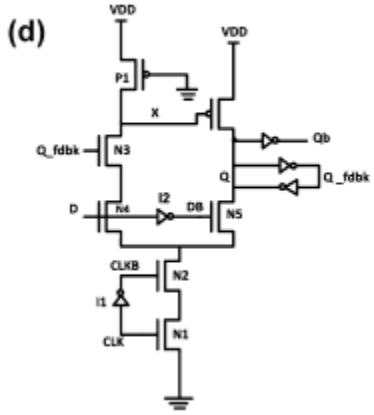
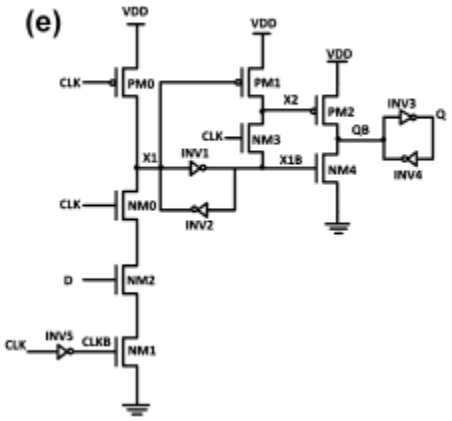


Fig. 1. Conventional flip-flop designs. (a) Semi-dynamic flip-flop (SDFF) [14]. (b) High speed dual-edge triggered modified HLFF (HSDMHFF) [15]. (c) Dynamic explicit pulsed triggered flip-flop (DEPFF) [16]. (d) Single-ended conditional capturing energy recovery flip-flop (SCCER) [17]. (e) Dual dynamic node flip-flop (DDFF) [18].





It is useful to noting that some works have been devoted [24–26] to develop circuital techniques to design efficient flip-flops. For example in [24], a new framework developed a power and speed efficient method to greatly avoid the detrimental effects corre-spond to current contention mechanisms, occurring at critical switching nodes of pulse triggered flip-flops [24]. Note that another FF which is based on the C-element is C-element dual data rate (C-DDR) flip-flop [27], but its large positive setup time limits its speed because of circuit structure, and herein is ignored from the comparisons.

3. Proposed design

Prior to explaining the structure and functionality of proposed design, the operation of C-element which has two inputs and one output is described: If two inputs of a C-element are similar, C-element output will be inverted of inputs; otherwise C-element keeps the previous value [28]. Both schematic and timing diagram of proposed flip-flop are shown in Fig. 2. This scheme is called hybrid pulsed flip-flop since dynamic front-end stage and a static output one are employed in the circuit. This proposed design, as shown in Fig. 2(a), constitutes of three parts: (1) sampling circuit made up from five transistors, i.e., transistors M1-M2, as well as inverter I1; (2) a simple C-element having four transistors, i.e., M3-6; (3) a keeper (Inverter pair I3-4). Referring to Fig. 2(a), nodes X and DB (complementary input data) are as inputs of the C-element. Firstly, if the input data is low, as seen in the timing diagram in Fig. 2(b), when the rising edge of clock arrives, transistor M2 is on and signal CLKB remains high to turn on transistor M1 for a short period time, i.e., transparency window, and shown in rectangle in Fig. 2(b). Therefore, M1–M2 are both on during this short time slot. If a “1” to “0” data transition occurs, DB becomes 1, M1 and M2 pass DB to node X which will be precharged to turn on both M5 and M6 through which

node Q is pulled down. The transparency window is shut down as CLKB is low. Analogously, when input data is high or makes a transition from "0" to "1", DB becomes low. As mentioned, when the rising edge of clock comes, M1–M2 are turned on tem-porarily to sample data, and driving node X pull down through this route. Since C-element output is high if its two inputs are both low, node Q becomes 1, bringing QB to low. Indeed, at Inverter I1, similar to [23,29], transistor M7 with VDD input is employed in series with pull-down network of I1 for implementing sufficient delay for this stage.

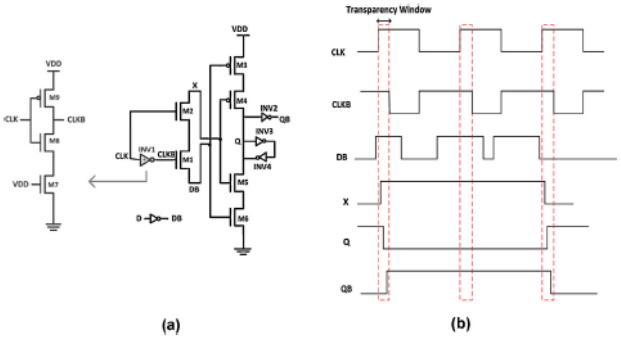


Fig. 2. Proposed flip-flop: (a) schematic; (b) timing diagram

What is important in functionality of a FF is to have no output voltage changing at the clock level, and this FF is only sensitive to rising edge of clock because if D changes in the clock level, node X keeps its previous value as either M1 or M2 transistor does not operate, thus nodes DB and X have different values and there are no paths to copy DB into X, i.e., C-element retains previous value, which holds the output stage of FF. Thereby, there is no signal switching in any internal nodes. It guaranties that proposed FF is not sensitive to the clock level as should be expected. This FF contains only 17 transistors making it appropriate for low area. As described in timing diagram in Fig. 2(b), no transitions occurs in internal nodes at every clock cycle unless D invokes output changes, reducing power dissipation owning to no dynamic power dissipation at its internal nodes in these states. This technique named conditional transition.

It should be mentioned that if we used node D instead of node DB in M1 source, it would pose an issue to some extent since glitches of node X can be present on the input data directly, causing noise susceptibility increases whereas use of DB prevents this problem completely; thus, M1 source must be connected to DB.

4. Simulation results

To follow real environment and to obtain the realistic associated performance of the all FFs, input buffers were inserted so as to drive FF inputs, and output must drive a load. Flip-flops were designed in 45 nm CMOS technology with a 1 V supply voltage using Virtuoso. The output load capacitor of FF is 30 ff while clock frequency is 1 GHz for single-edge triggered FFs and 500 MHz for dual-edge triggered ones. Furthermore, an extra capacitor whose value is 2 ff is inserted after clock buffer. The sweeping the "0" to "1" and "1" to "0" data transition times with respect to the clock edge, D-to-Q delay is obtained, and minimum data-to-output delay defines optimum setup time [30,31]. Simulated waveform is illustrated in Figs. 3. The minimum delay D-to-Q and power consumption of proposed design is lower than that of others, because using the conditional transition mechanism along with number of four clocked transistors make proposed flip-flop well-suited in terms of power dissipation at all activity factors. Also, presented design requires the fewest transistors among its counterparts due to its circuitry simplification and mechanism novelty.

Setup and hold times are parameters for which there are two different definitions. In this work, an interval time between CLK and data which causes optimum D-to-Q delay is defined as setup-time, whereas maximum time that input data must be stable after clock edge in order that flip-flop capture the correct data denotes hold time [18,32].

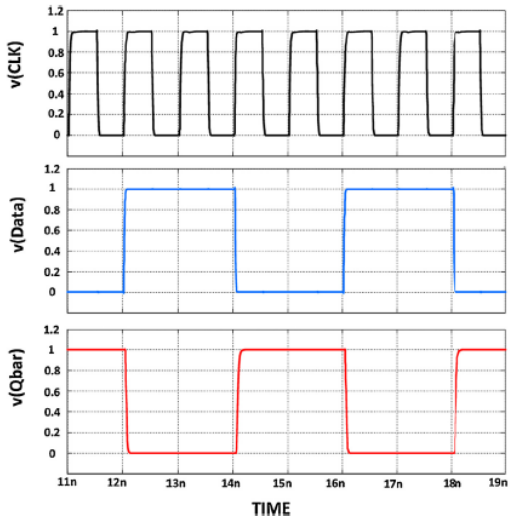


Fig. 3. Simulated waveforms of proposed design

5. Conclusions

In this paper, a new implicit-pulse triggered flip-flop was presented, which is a pulsed hybrid type one. There were only four clocked transistors which results in significant power saving. The key idea was exploitation of a C-element for which two input signals were provided via input data and common node of two series pass transistors. Therefore, the correct value of output was obtained and held by a simple

latch. All flip-flops were implemented in 45 nm technologies, and experimental results show that the average saving in power consumption in 50% data activity and delay are 16.9% and 5%, respectively. Moreover, proposed circuit has the least power consumption at all data activities. In all process corners, it has superior power-delay-product saving.

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