Reduced Device count 7-Level Asymmetrical Multilevel Inverter with Various Modulation Schemes

Jyoti Tomar , Kuldeep Swarnkar , Praveen Bansal

***Abstract*-Multilevel inverters offers various applications in voltage ranging from medium to high such as in renewable sources, industrial drives, blowers, conveyors and fans. Multilevel inverters are key technology in various industries operations and becoming more and more popular day by day because of its many advantages over 2-level inverter such as less THD in output waveform, voltage stress on switches and less electromagnetic interference. This paper presents a new asymmetrical MLI topology for 7-level inverter which require less number of switches and driver circuits as compared to other conventional MLI topologies. This proposed MLI topology here is implemented with different pulse width modulation techniques, which requires less amount of power switches and voltage sources to reduce the complexity of circuit as compared to other MLI configurations. MATLAB/Simulation is used to simulate the results of 7-level MLI inverter topology.**

Index Terms - Multilevel inverter (MLI), seven level inverter, asymmetric topology, total harmonic distortion (THD), multicarrier pulse width modulation.

I.INTRODUCTION

A multilevel inverter is a power electronic device which is capable of providing desired alternating voltage level at the output using multiple lower level DC voltages as an input. Mostly a two-level inverter is used in order to generate the AC voltage from DC voltage. Multilevel Inverters have come upon with broad applications, especially high power and medium voltage drives, distributed generation, HVDC transmission, static VAR compensation, electric vehicular technology and many more [1-2]. The main advantage of multilevel inverter over two level inverters configurations are decrease total harmonic distortion (THD), decrease dv/dt stress across devices, less electromagnetic interference (EMI), less common mode voltage and improve use of rail voltage etc.

Several multilevel topologies have been classified as the diode clamped multilevel inverter (DCMLI) [2], the flying capacitor multilevel inverter (FCMLI) [3], the cascaded H-bridge multilevel inverter (CHBMLI) [4]. The diode clamped and flying capacitor converter configurations function with the single DC source but the number of device increase parabolically with the number of output levels raises production cost and complicated control. In cascaded H-bridge multilevel inverter uses full H-Bridge connected in series to produce inverter AC from separated DC sources but major disadvantage is requirement of multiple DC – sources, which is not feasible in many applications. In Multilevel inverters the basic principle is to use low voltage switches for getting high output voltage by dividing the supply voltage among the power electronics switches. An asymmetric topology [5] is presented which uses one voltage sources and two switches are the basic unit. One more dc voltage source and a switch is connected with the basic unit to generate more level in output voltage. These units are connected in series in order to achieve more levels. Usage of unidirectional and bidirectional switches makes the multilevel inverter of large size.

The proposed topology [9] consists of two dc voltage source and six power electronic switches. This topology is compared with various topologies to show its advantages. The proposed is stimulated in MATLAB for 7-level inverter. It can also be used for three phase system.

II. PROPOSED TOPOLOGY AND ITS OPERATION

A new topology for 7-level base on asymmetrical multilevel inverter is shown in Fig.1. It consists of six power electronic switches written as Sw_1, Sw_2, Sw_3, Sw_4, Sw_5, Sw_6 and two dc voltage sources of different rating named as V_1 and V_2. Out of six switches two switches are bidirectional (Sw_2, Sw_6) and other four switches are unidirectional (Sw_1, Sw_3, Sw_4, Sw_5).

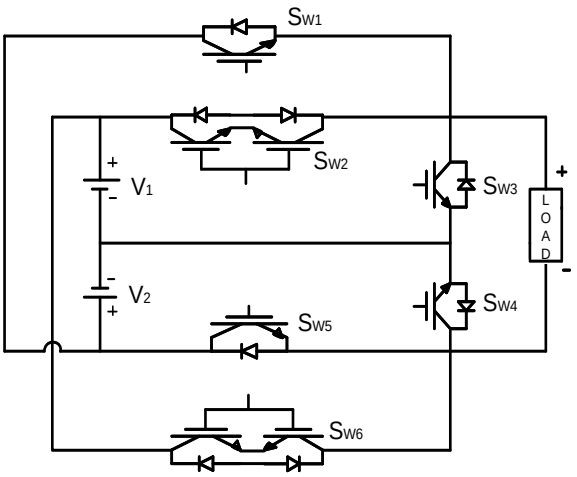

Fig. 1.1 Proposed seven level inverter

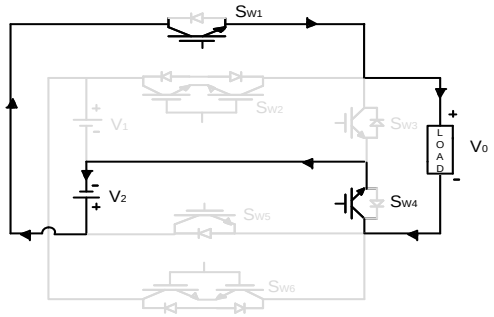

Fig.1.2(a) Mode 1; V0 = 3V1

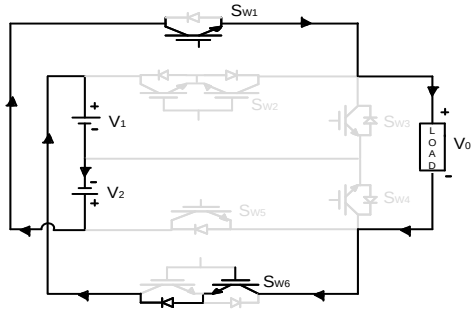

Fig.1.2(b) Mode 2; V0 = 2V1

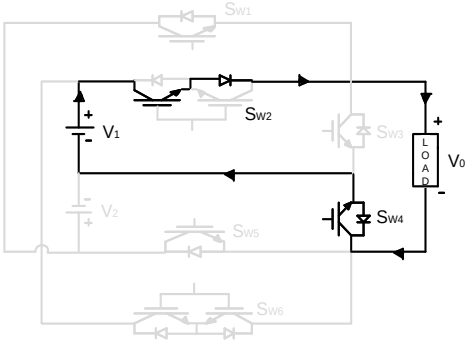

Fig.1.2(c) Mode 3; V0 = V1

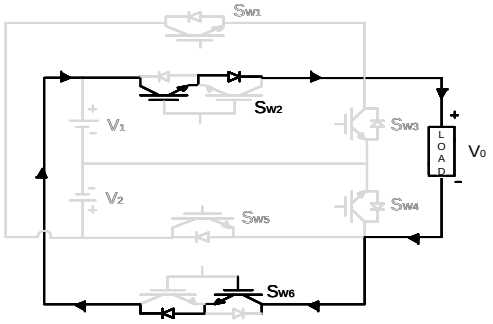

Fig.1.2(d) Mode 4; V0 = 0

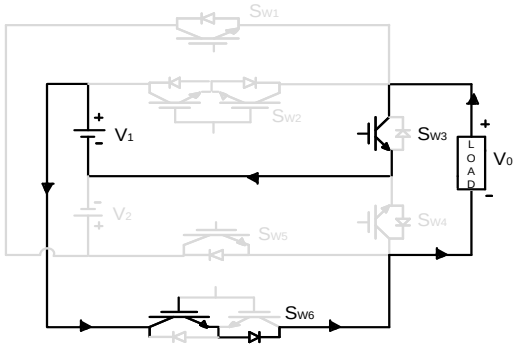

Fig.1.2(e) Mode 5; V0 = -V1

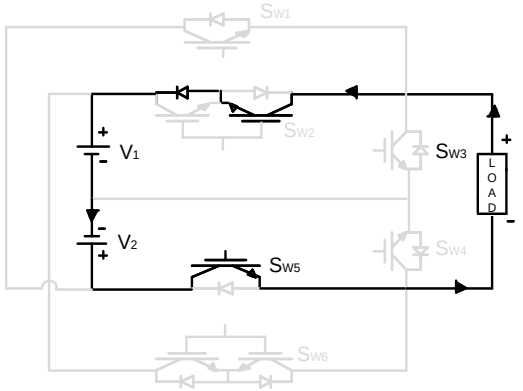

Fig.1.2(f) Mode 6; V0 = -2V1

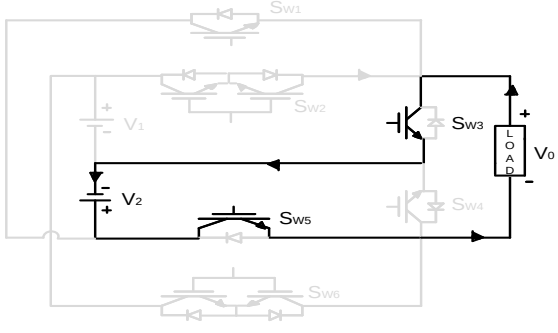

Fig.1.2(g) Mode 7; V0 = -3V1

The bidirectional switches can conduct current and block voltage in both the directions. To achieve all seven level voltage, the values of dc voltage source V1 and V2 should be in the ratio 1:3.

Mode 1: When switches SW1 and SW4 are turned ON, output voltage will be equal to 3V1.

Mode 2: When switches SW1 and SW6 are turned ON, the output voltage will be given by 2V1 (V2-V1).

Mode 3: When switches SW2 and SW4 are turned ON, the output voltage will be V1.

Mode 4: When switches SW2 and SW6 are turned ON, the output voltage will be 0.

Mode 5: When switches SW3and SW6 are turned ON, the output voltage will be -V1.

Mode 6: When switches SW2 and SW5 are turned ON, the output voltage will be -2V1.

Mode 7: When switches SW3and SW5 are turned ON, the output voltage will be -3V1.

The following seven level voltage is obtained:

(3V1, 2V1, V1, 0, -V1, -2V1, -3V1)

Table I. Look up table for various operating modes:

Level of output voltage	Switch States					
	SW1	SW2	SW3	SW4	SW5	SW6
3V1	✓			✓		
2V1	✓					✓
V1		✓		✓		
0		✓				✓
-V1			✓			✓
-2V1		✓			✓	
-3V1			✓		✓	

III.MULTICARRIER PWM TECHNIQUES[6-8]

Carrier Disposition techniques-

1. Phase Disposition (PD) Technique
2. Phase Opposition Disposition (POD) Technique
3. Alternate Phase Opposition Disposition (APOD) Technique
4. Inverted Sine Carrier PWM (ISCPWM) Technique

PD, APOD, POD techniques are multicarrier PWM schemes having triangular carrier whereas reference is also sine wave .In ISCPWM carrier is sine of constant frequency and reference is also sine wave .

- **PHASE DISPOSITION TECHNIQUE**

  In PD technique all carrier waveform are superimposed over one another like layer with same phase, amplitude and frequency as shown in Fig 3.1

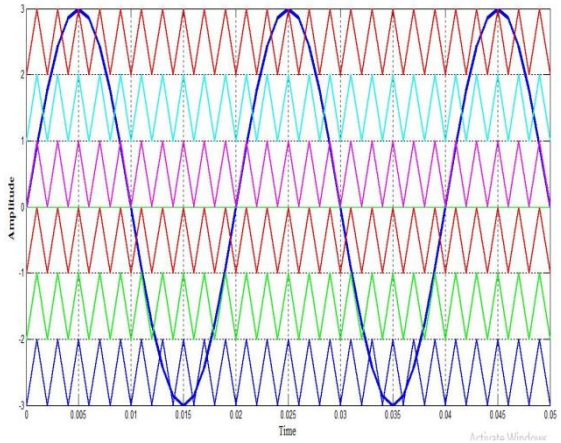

Fig.3.1 Phase disposition technique

- **PHASE OPPOSITION DISPOSITION TECHNIQUE**

  The carrier waveform are all in phase above and below the zero reference value however, there is 180 degree phase shift between the ones above and below zero respectively as shown in Fig.3.2

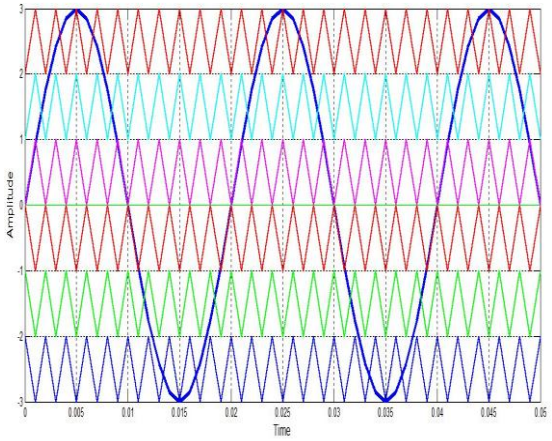

Fig.3.2 Phase opposition technique

- **ALTERNATE PHASE OPPOSITION DISPOSITION TECHNIQUE**

  In APOD technique all the adjacent carriers are 180 degree out of phase from each other on either side of zero reference level as shown in Fig 3.3

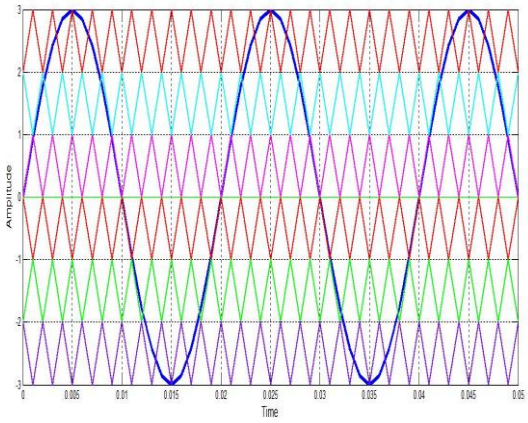

Fig.3.3 Alternate phase opposition disposition technique

- **INVERTED SINE CARRIER PWM TECHNIQUE** In ISCPWM technique inverted sine wave of certain constant frequency acts as a carrier signal as shown in Fig 3.4

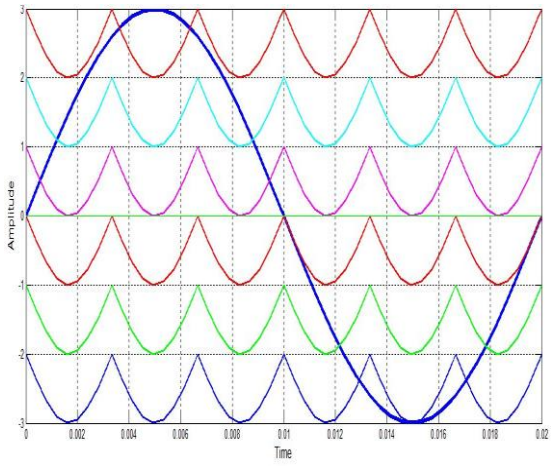

Fig.3.4 ISCPWM Schemes

IV.SIMULATION RESULT

Output voltage wave and Current waveform of seven level inverter shown in Fig.4.1 and Fig.4.2 respectively.FFT analysis for various modulation schemes is shown from Fig.4.3 to Fig.4.5 and it can be seen that THD is lowest by PD technique which is 14.30% at modulation index(m_a=1).In APOD and POD technique THD is higher i.e. 14.73% and 15.50% respectively.THD is low in PD technique hence switching loss and power loss is less consequently efficiency is high and cost is reduced considerably.

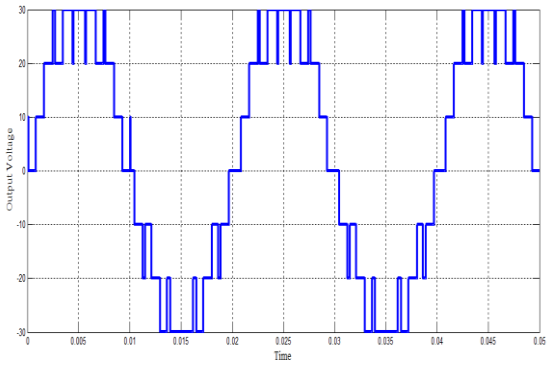

Fig.4.1Output voltage waveform

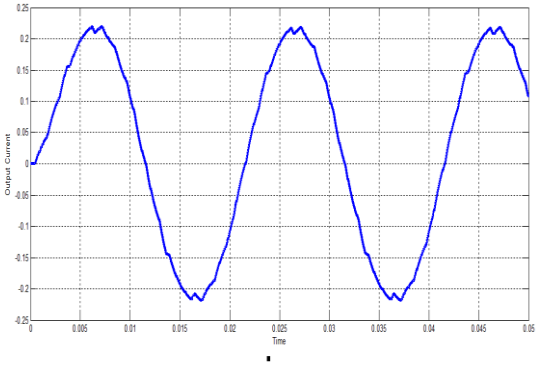

Fig.4.2 Output current waveform

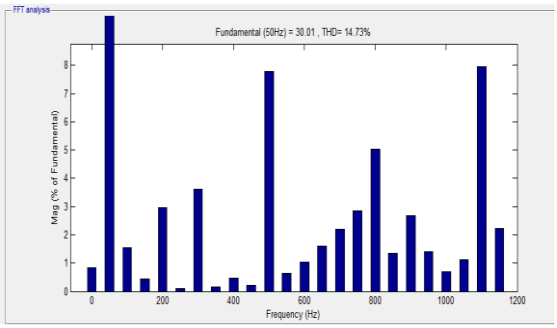

Fig.4.3 FFT Analysis of APOD(m_a=1)

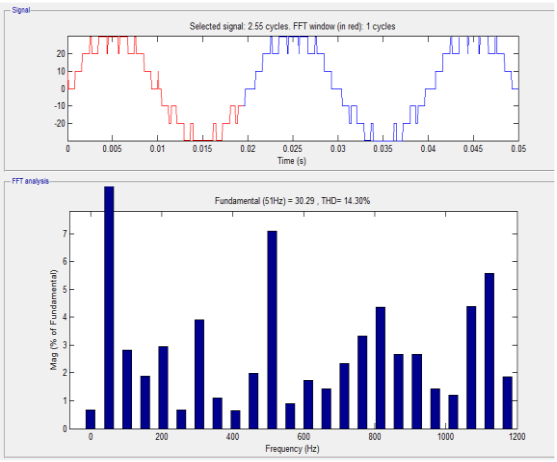

Fig.4.4 FFT Analysis of PD(m_a=1)

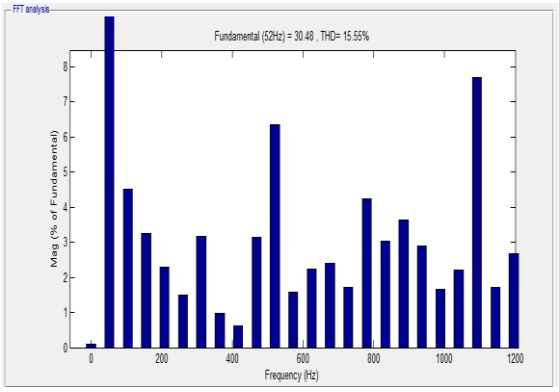

Fig.4.5 FFT Analysis of POD(m_a=1)

Table. II Indicating THD(%)for various modulation schemes at different modulation indices

SCHEMES	**MODULATION INDICES**			
	1	**0.95**	**0.9**	**0.85**
PD	14.30	15.78	16.67	15.54
POD	15.50	16.98	17.87	16.65
APOD	14.73	15.02	15.76	16.04
ISCPWM	15.67	17.89	18.56	17.45

Table.III Comparison of conventional topologies with proposed topology

Topology	Diode Clamped	Flying Capacitor	Cascaded H-Bridge	Proposed Topology
Clamping Diodes	30	0	0	0
Floating Capacitor	0	15	0	0
Switches (Main)	12	12	12	6
Input DC source	1	6	3	2
Total IGBT	12	12	12	8

V.CONCLUSION

It can be concluded that proposed topology offer reduced count of switches in comparison to conventional topologies. Filter requirement is reduces as lower order harmonics are reduced and switching losses reduced which renders high efficiency and low cost. Proposed topology offers greater advantage as it is less bulky that other topologies. Hence it can be concluded that proposed topology is superior than conventional inverters.

VI. ACKNOWLEDGMENT

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