A Power Effective Asymmetric Topology for 7-Level Multilevel Inverter with Different PWM Techniques

Deepak Singh, Praveen Bansal

Abstract:- The need of multi-level inverter has been expanded owing to their high power applications and the capability for getting almost a sinusoidal output voltage liken to conventional two level inverter. This paper orient to develop a new variety of asymmetric multilevel inverter configuration for generations of seven levels of output voltage.
This proposed multilevel inverter topology here is implemented with different pulse width modulation (PWM) techniques, which requires less count of power switches and voltage sources to reduce the complexity of a circuit as compare to other multilevel inverter configurations. A multicarrier PWM technique is used to generate 7-level output phase voltage. MATLAB/simulation is used to simulate the results of a 7-level multilevel inverter topology.

Keywords- multilevel inverter (MLI), seven level inverter, asymmetric topology, total harmonic distortion (THD), multicarrier pulse width modulation.

I. INTRODUCTION

In recent years with the enhancement of power semiconductor engineering, multilevel inverter (MLI) have obtained tremendous popularity among researches as well as in industries owing to use in high power and high voltage applications [7]. The first use of the word " multilevel inverter " was recorded in year 1970s and 1980s. The basic of a multilevel inverter is called three level. It is similar to a square wave form [3]. The major areas of application multilevel invertor are : high power medium voltage drives, HVDC transmission, distributed generations, electrical vehicular technology, static VAR compensator, induction heating, stand by air – craft power supplies, UPS (uninterruptable power supplies) for computer[2]. The main advantage of multilevel inverter over two level inverters configurations are decrease total harmonic distortion (THD), decrease dv/dt stress across devices, less electromagnetic interference (EMI), less common mode voltage and improve use of rail voltage etc [4].
Several multilevel topologies have been classified as the diode clamped multilevel inverter (DCMLI), the flying capacitor multilevel inverter (FCMLI), the cascaded H-bridge multilevel inverter (CHBMLI) [6]. The diode clamped and flying capacitor converter configurations function with the single DC source but the number of device increase parabolically with the number of output levels raises production cost and complicated control. In cascaded H-bridge multilevel inverter uses full H-Bridge connected in series to produce inverter AC from separated DC sources but major disadvantage is requirement of multiple DC – sources, which is not feasible in many applications. This paper present a new 7-level topology of asymmetrical multilevel inverter configuration in section II, using fixed frequency level shifted carrier based pulse width modulation techniques which require for decrease deformation of sinusoidal voltage and less number of power switches. The operations with & operating is addressed in section III, section IV describes multi carrier PWM techniques, the simulated result of proposed MLI shows in section V, relevant conclusion are given in section VI.

II. PROPOSED TOPOLOGY

The aim of this topology is to provide a uncomplicated construction from the perspective of design and control, minimizes power system losses and ensure a less total harmonic distortion, which may have a positive effect on the employed AC side filter. As shown in figure 2.1, the seven- level structure contains only voltage sources and switches (unidirectional S1, S2, S3, S4 and bidirectional S5, S6). This would be the wide gain over some topologies usable in the literature which use extra diodes or may be transformers [8] to clamp or lift the voltage up to a suitable level. These composite topologies, still display some difficulty partially related to the transformer core losses and to the diode peak reverse recovery current, that largely gains the switch turn-on losses and as well drives high voltage spikes in inductive loads due to the high di/dt. The magnitude of dc voltage sources are V1 = 50v and V2 = 100v. The value of output voltage frequency is 50 Hz. The R-L load of R= 110Ω, L= 160mH. TABLE 1 shows the value of output voltages (V0) for the different states of S1, S2, S3, S4, S5 and S6 switches.

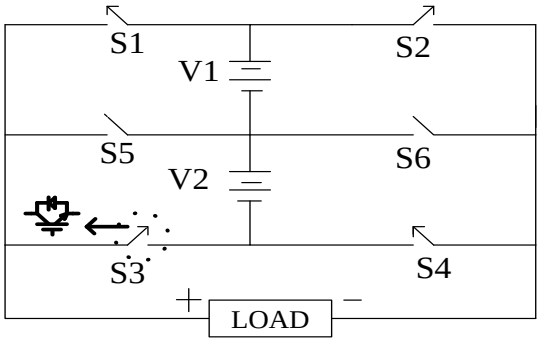

Fig 2.1 Asymmetric multilevel inverter

TABLE 1

Switching States For 7-Level Asymmetric MLI

V0	SWITCHING STATE (1 = ON)					
	S1	S2	S3	S4	S5	S6
+150	1			1		
+100				1	1	
+50	1					1
0	1	1				
-50		1			1	
-100			1			1
-150		1	1			

III. OPERATING MODES

Various operating modes to obtain different voltage are shown in the following figures.

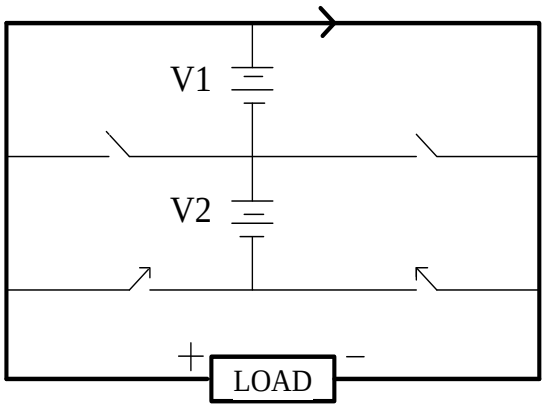

Fig 1 ; V0 = 0v

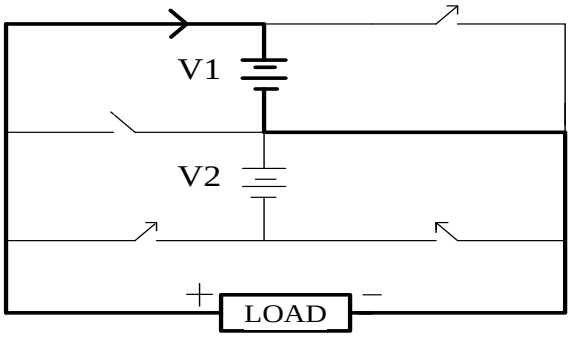

Fig 2 ; V0 = 50v

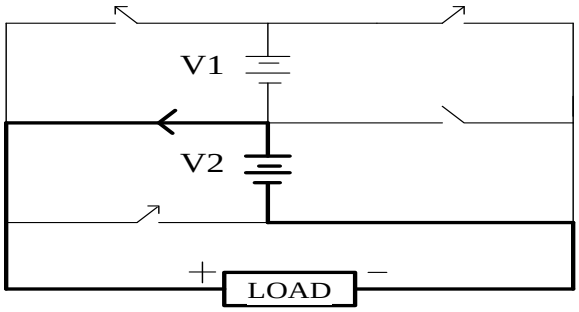

Fig 3 ; V0 = 100v

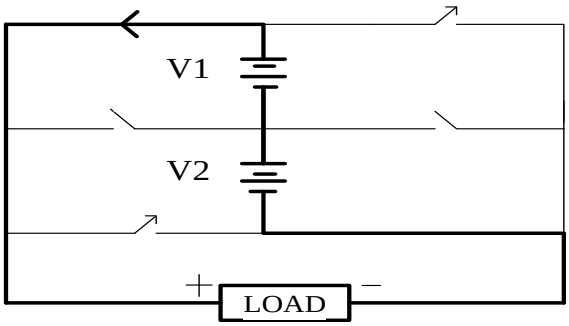

Fig 4 ; V0 = 150v

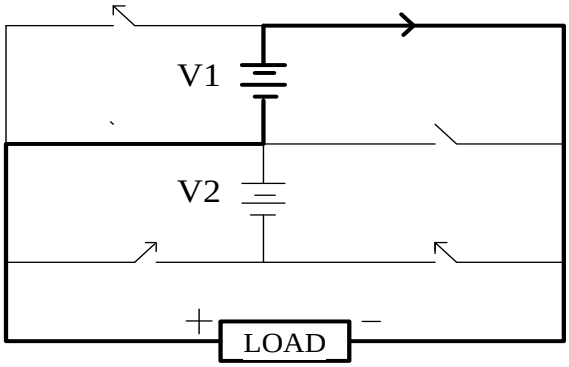

Fig 5 ; V0 = -50v

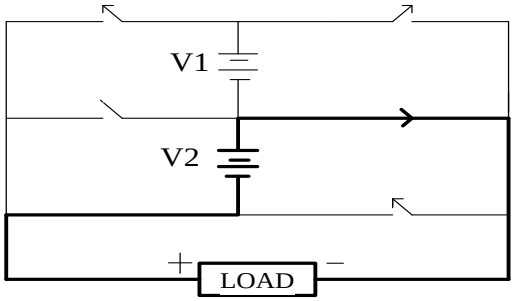

Fig 6 ; V0 = -100v

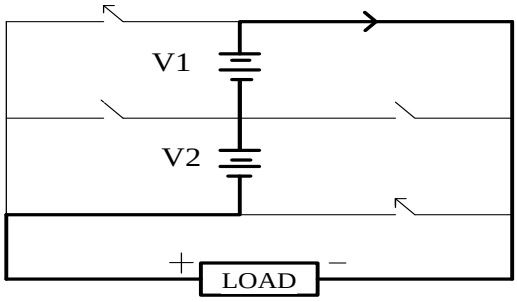

Fig 7 ; V0 = -150v

IV MULTICARRIER PWM TECHNIQUES

Carrier Disposition techniques-

a) Phase Disposition(PD)
b) Phase Opposition Disposition(POD)
c) AlternatePhaseoppositionDisposition(APOD)
d) Inverted sine carrier PWM(ISCPWM)

- PHASE DISPOSITION TECHNIQUE

In PD technique all carrier waveform are superimposed over one another like layer with same phase, amplitude and frequency as shown in figure 4.1

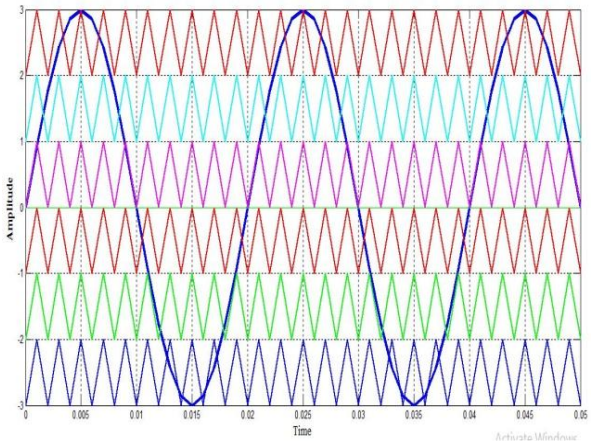

Fig 4.1

- PHASE OPPOSITION DISPOSITION TECHNIQUE

In POD technique the carrier waveforms above or below the zero reference are phase shifted by 180 degree as shown in figure 4.2

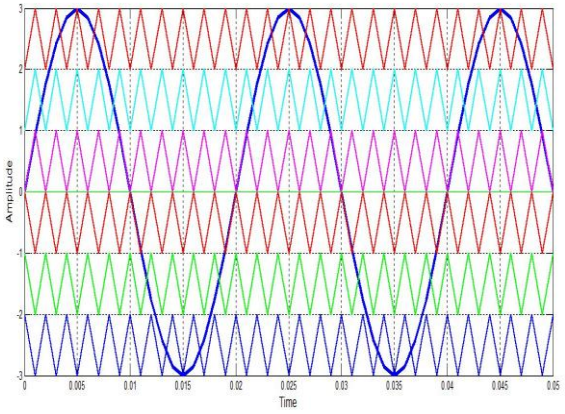

Fig. 4.2

- ALTERNATE PHASE OPPOSITION DISPOSITION

In APOD technique all the adjacent carriers are 180 degree out of phase from each other on either side of zero reference level as shown in figure 4.3

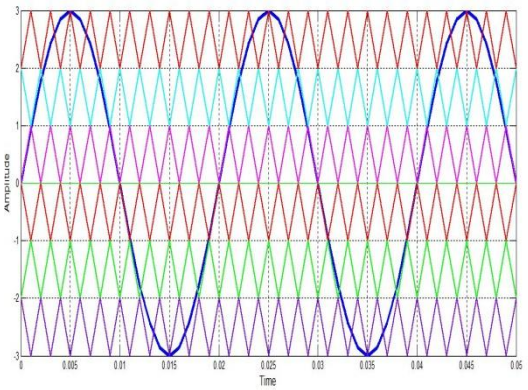

Fig. 4.3

- INVERTED SINE CARRIER PULSE WIDTH MODULATION TECHNIQUE

In ISCPWM technique inverted sine wave of certain constant frequency acts as a carrier signal as shown in figure 4.4

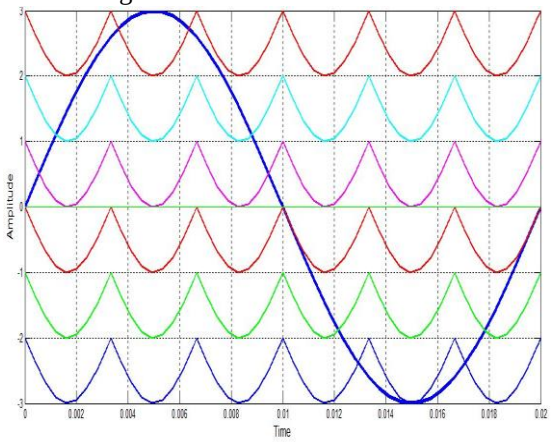

Fig 4.4

V. SIMULATION RESULT

A elaborated circuit simulation has been done to present the operating principle of a 7-level topology of asymmetrical multilevel inverter configuration. Fig.5.1, 5.2 shows the simulated output voltage and load current waveform respectively of proposed inverter.

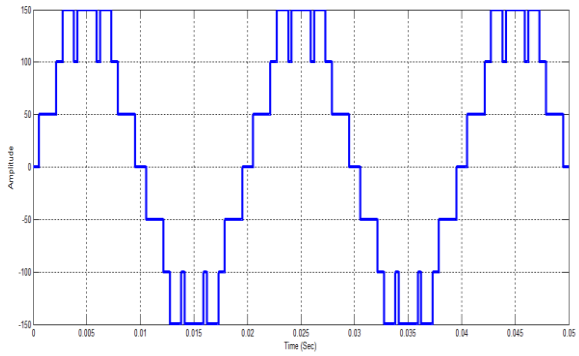

Fig. 5.1 Output Voltage Waveform

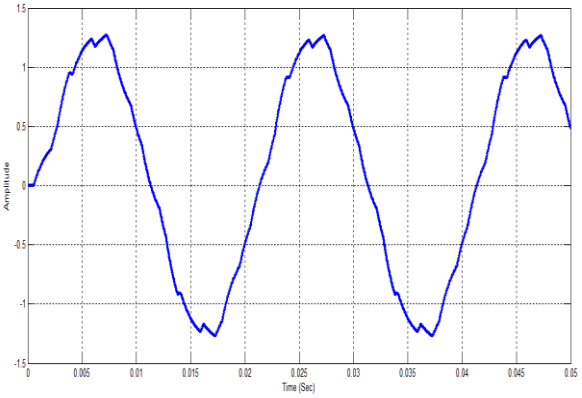

Fig. 5.2 Output Current Waveform

Figure shows FFT analysis of proposed inverter for Ma=0.9 and Mf=20 respectively by POD, PD, APOD PWM technique and for Ma=1 by ISCPWM technique.

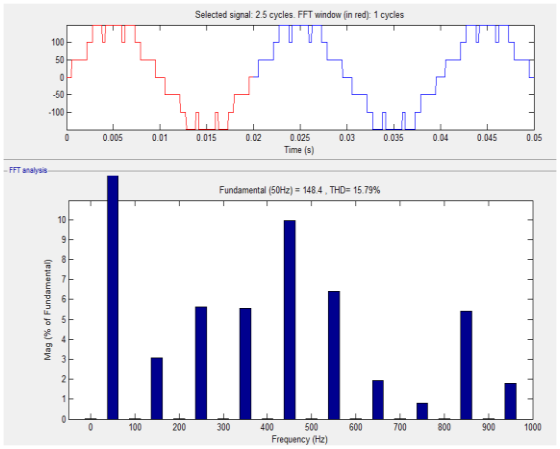

Fig. 5.3 FFT analysis by PODPWM

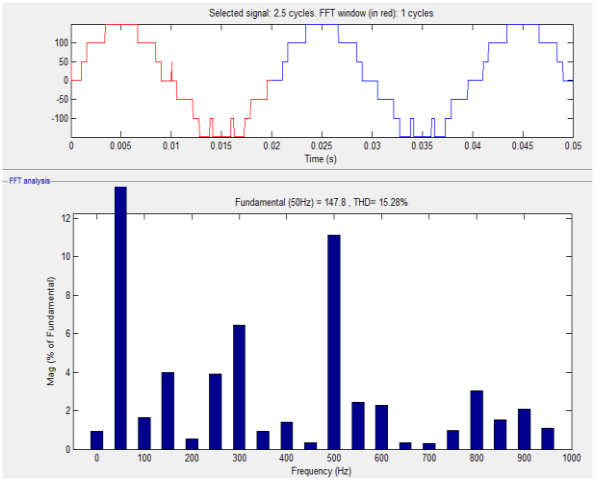

Fig. 5.4 FFT analysis by PDPWM

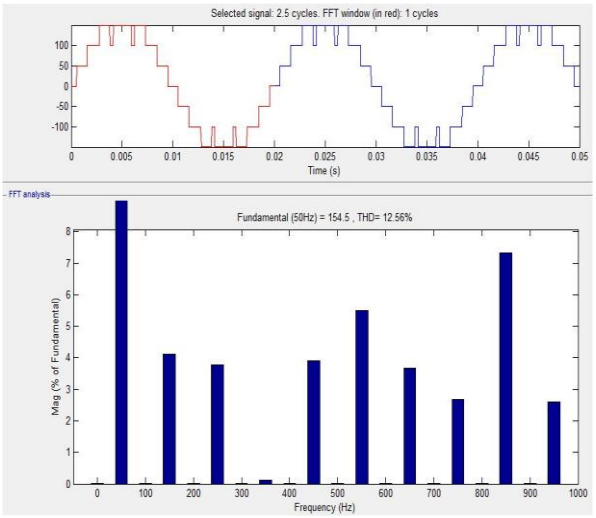

Fig. 5.5 FFT analysis by APODPWM

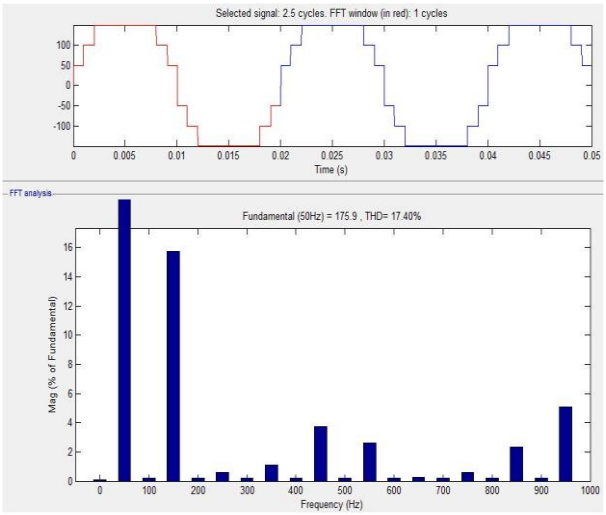

Fig. 5.6 FFT analysis by ISCPWM

TABLE II

THD analysis for various modulation techniques

Technique	**Modulation index**			
	1	**0.95**	**0.9**	**0.8**
PD	15.28	17.85	19.19	19.76
POD	15.79	19.27	19.47	19.76
APOD	12.56	17.20	18.27	18.32
ISCPWM	20.87	20.14	19.13	17.40

TABLE III
Comparison between different MLI topologies

Topology	Diode Clamped	Flying Capacitor	Cascaded H-Bridge	Proposed Topology
Clamping Diodes	30	0	0	0
Floating Capacitor	0	15	0	0
DC-link Capacitors	6	6	0	2
Switches (Main)	12	12	12	8
Input DC source	1	1	3	2

VI. CONCLUSION

In this paper, a 7-level asymmetric multi-level inverter power effective topology is proposed with different PWM techniques and proposed MLI topology with different PWM techniques is used to generate 7-level output phase voltage. It is proved that, the proposed work of Single phase 7-level MLI output voltage total harmonics distortion is reduced and improve the efficiency of system compare with different conventional topologies of 7-level MLI. Harmonic analysis carried out using Mat Lab R2013a version software. This proposed MLI topology requires less number of components as compared to conventional MLI inverters. Simulation results show the performance of 7-level MLI with different PWM techniques.

VII. ACKNOWLEDGMENT

The author thankful to Electrical Engineering Department, Madhav Institute of Technology and Science, Gwalior ,India to the guidance and support for carrying out this work.

VIII. REFRENCES

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