Applications of Various Modulation Schemes In Symmetrical Seven Level Inverter Topology

[1]Ashwini Ojha,[2]Praveen Bansal

***Abstract*: In this paper a novel and efficient seven level multilevel inverter topology is introduced which produces seven output levels with reduced number of switches. As it has seven power switches so proposed inverter is less bulky and having additional advantages of highly efficiency, low switching losses and reduced cost. Various modulation schemes of multiple carrier type with high carrier frequency are employed on this proposed topology. On addition to this proposed topology is compared with conventional multilevel inverter topology. Performance parameter THD(Total harmonic distortion) is evaluated by MATLAB environment. Working of seven level inverter topology is carried out in MATLAB/Simulink and simulated results are further presented.**

***Keywords:* Multilevel inverter, pulse width modulation,POD,APOD**

I.INTRODUCTION

Nowadays Multilevel inverters are became popular within the power electronics field. [1-2]Two level inverters are failed to deal with consumer requirements like power quality and reliability. So MLIs are becoming popular as they are highly efficient and reliable.It became easy to generate a high power, high voltage inverter with the multilevel structure due to the way in which device voltage stresses are controlled inside the structure. Design of MLIs allows to reach staircase waveform of output voltage and hence reduces THD.With increment in number of levels Harmonics reduced considerable, hence efficiency increase and power loss reduced.[3] The conventional multilevel inverters can be classified into three types. They are 1) Diode clamped multilevel1 inverter(DCMLI) [4] 2) Flying capacitor multilevel inverter(FCMLI) [5] 3) Cascaded Hybrid Bridge multilevel inverter(CHBMLI)[6].These MLIs had been proposed long back but these topologies are bulky and offer more switching and ON state losses as switch count is higher than proposed symmetrical seven level topology.

In proposed topology three batteries are used of equal magnitude. Seven switches are used and they are operated such that they produces output voltage of seven levels. Basic unit is H-Bridge inverter and it is exploited in such a way that it produces maximum output levels however number of batteries are increased.THD for various modulation techniques will be presented are in conformity with MATLAB/Simulink environment.

II.PROPOSED MULTIEVEL INVERTER

The proposed topology is developed from[7] ,that can produce seven level of output voltage with decrement in count of number of power switches than conventional topology. Proposed topology is shown in Fig.1 which indicates two parts of inverter 1) Level generator 2)Polarity generator. In which level generator produces levels of output voltage and polarity generator.

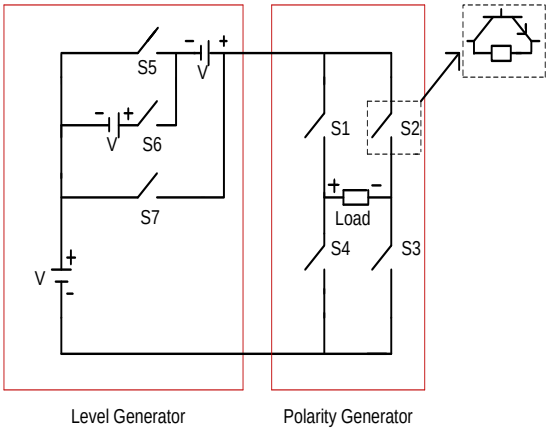

Fig.1 Proposed Inverter Topology

Proposed inverter topology produces staircase type of output voltage having output levels as V,2V,3V,0,-V,-2V AND -3V.More the levels of more is output wave near to sinusoidal waveform which essentially reduces THD hence powder loss decreases and efficiency increases. These levels as discussed will be obtained by proper operation of power switches as shown in Fig.1.

III.CIRCUIT OPERATION

Now circuit operation will be understood with relevant switching. To obtain level 1 i.e. V volt output switches are operated as follows S_7,S_1 and S_3 are ON as shown in Fig.2.Similarly to obtain 2V output i.e. level 2 switching operation is S_5,S_1 and S_3.For other levels switching is shown by relevant diagrams. It may be noted that to obtain 0 level of output two switching combination is possible out of which one can be redundant. By this possible switching combinations seven level of output voltage can be obtained.IGBT switch is employed as shown in Fig.1which is used for high switching frequency. Further various modulation schemes will be employed to ascertain THD of this seven level inverter. Operating modes of seven level inverter are shown and are as follows.

Level 1:

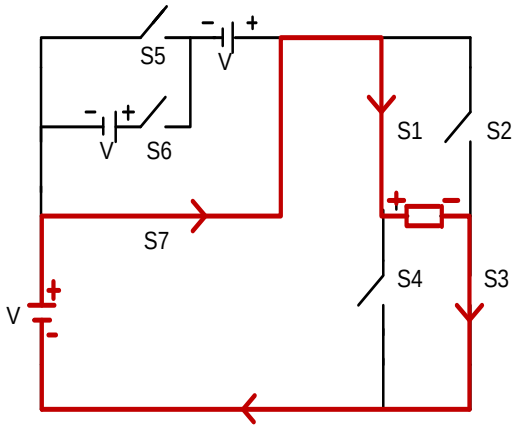

Fig.2 Switching combination for output voltage level of V

Level 2:

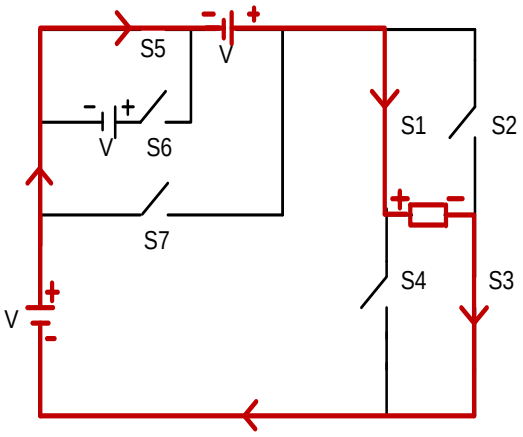

Fig.3 Switching combination for output voltage level of 2V

Level 3:

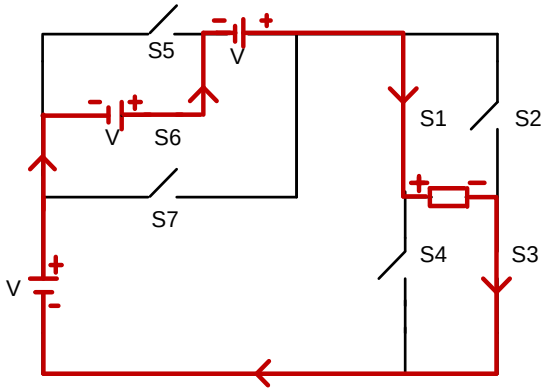

Fig.4Switching combination for output voltage level of 3V

Level 0:

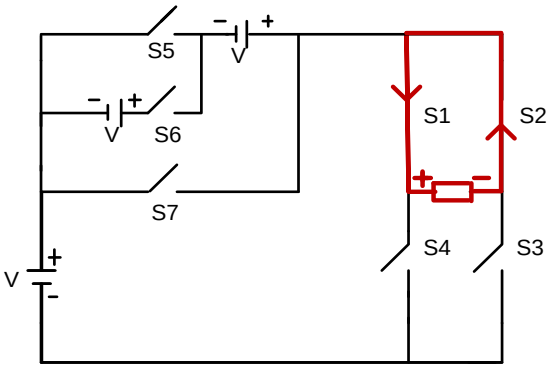

Fig.5 Switching combination for output voltage level of 0V

Level 0:

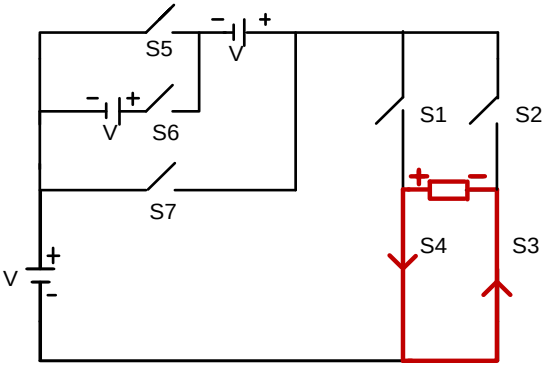

Fig.6Switching combination for output voltage level of 0V

Two switching combinations for 0 level of output is evident as load can be shorted in two ways i.e. by operating switches as follows$S_1$and S_2 in Fig.5.In Fig.6 switches S_3 and S_4 are operated to short the load such that output voltage is at 0 level. Out of these two levels one is redundant.

Level -1:

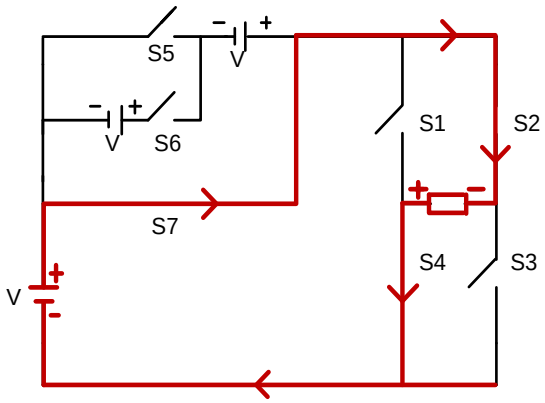

Fig.7 Switching combination for output voltage level of –V

Level -2:

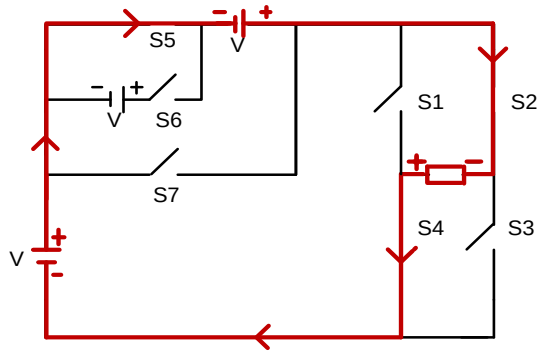

Fig.8Switching combination for output voltage level of –2V

Level -3:

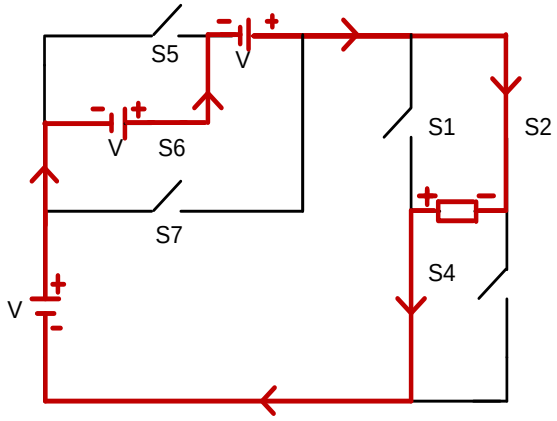

Fig.9Switching combination for output voltage level of –3V

In next section applications of various modulation techniques will be discussed in details. These modulation schemes ascertain THD. Third harmonic component can also be ascertained through FFT analysis if third harmonic component is reduced then filter requirement will be reduced as well as structure will not bulky.

Table I Switching states for seven level inverter

	States of switches (1=ON.0=OFF)						
Level	S_1	S_2	S_3	S_4	S_5	S_6	S_7
0	**1**	**1**	**0**	**0**	**0**	**0**	**0**
0	**0**	**0**	**1**	**1**	**0**	**0**	**0**
1	**1**	**0**	**1**	**0**	**0**	**0**	**1**
2	**1**	**0**	**1**	**0**	**1**	**0**	**0**
3	**1**	**0**	**1**	**0**	**0**	**1**	**0**
-1	**0**	**1**	**0**	**1**	**0**	**0**	**1**
-2	**0**	**1**	**0**	**1**	**1**	**0**	**0**
-3	**0**	**1**	**0**	**1**	**0**	**1**	**0**

IV.MULTI CARRIER PWM TECHNIQUES[8-10]
Carrier shifting techniques:

a) Phase Disposition (PD)
b) Phase Opposition Disposition (POD)
c) Alternate Phase opposition Disposition(APOD)
d) Inverted sine carrier PWM (ISCPWM)

Among these techniques PD,APOD,POD are multi carrier PWM schemes in which reference is sinusoidal and carrier is triangular. Whereas in ISCPWM carrier and reference both are sinusoidal.

These techniques will be discussed further with relevant waveform as follows:

- PHASE DISPOSITION (PD)
  In this technique each carrier is shifted amplitude wise from one other by 1.All the carriers are in same phase as shown in Fig.10.

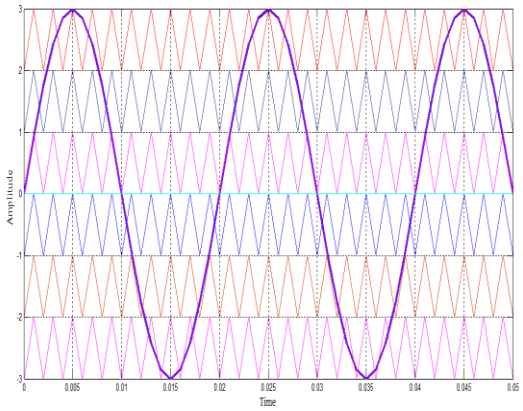

Fig.10 Phase Disposition technique

- PHASE OPPOSSITION DISPOSITION (POD)

  In this technique carrier above and below zero level are in phase and shifted from each other by 1.Carrier above and below zero level are 180 degree phase shifted.

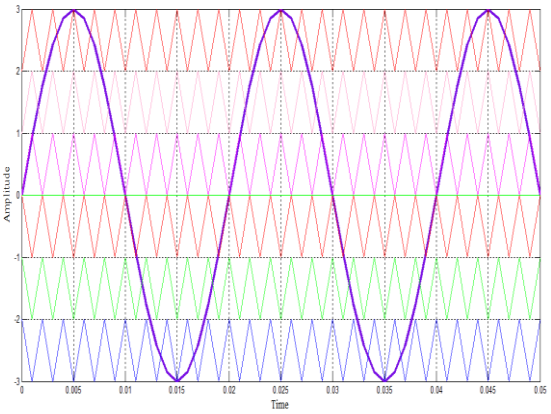

Fig.11 Phase opposition Disposition Technique

- ALTERNATE PHASE OPPOSSITION DISPOSITION (APOD)

  In this technique carrier wave is alternatively 180 degree phase displaced from each other as shown in Fig.

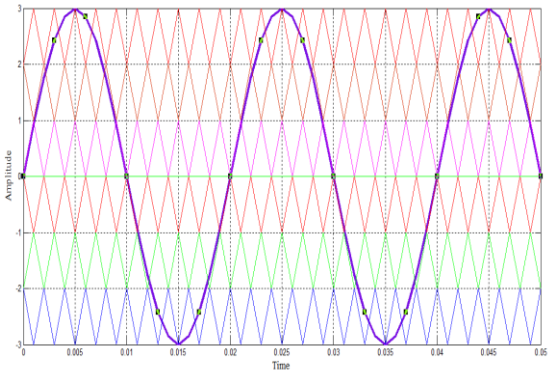

Fig.12 Alternate Phase opposition Disposition technique

- INVERTED SINE CARRIER PULSE WIDTH MODULATION(ISCPWM) TECHNIQUE

  In this technique carrier is inverted sine wave having constant frequency and reference is sine wave ,pulse will only be obtained when reference wave amplitude is more than carrier wave amplitude.

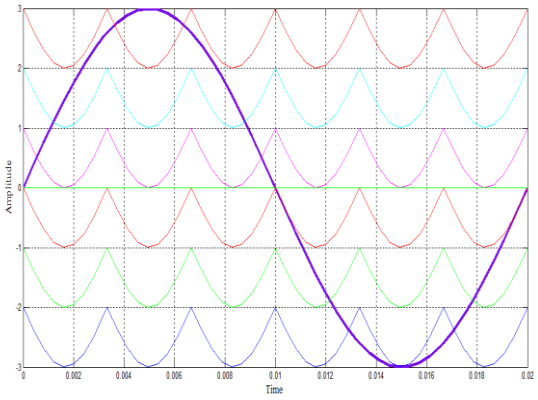

Fig.13Inverted sine carrier pulse width modulation technique

V.SIMULATION RESULTS

THD indicates harmonic contents in output voltage waveform of inverter and it is very popular parameter to assert quality of inverter. From Fig.14 to Fig.17 FFT analysis is shown and it can be easily asserted that POD technique offers least THD of 14.57% at modulation index (m_a) of 1.PD technique offers THD of 15.48% and APOD offers THD of 17.15% and third harmonic content is increased considerably at m_a equals to 1.ISCPWM technique offers THD of 16.07% and third harmonic is less than APOD.Battery voltage is chosen 100 V for all the batteries.

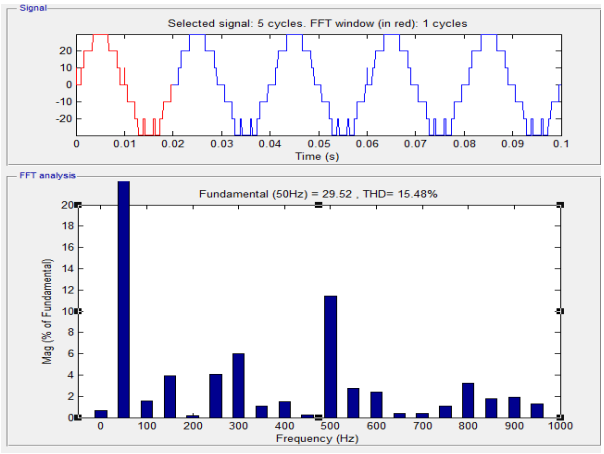

Fig.14 FFT analysis of PD technique for m_a=1

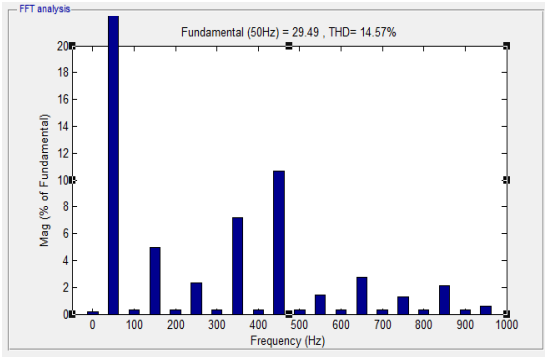

Fig.15 FFT analysis of POD technique for m_a=1

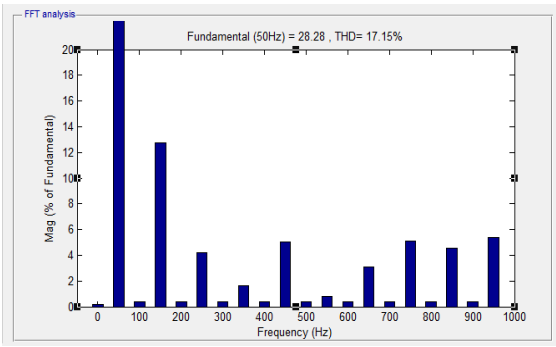

Fig.16 FFT analysis of APOD technique for ma=1

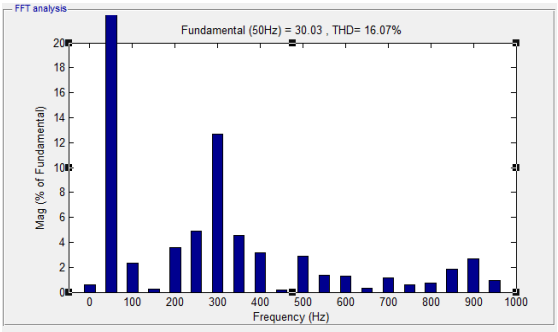

Fig.17 FFT analysis of ISCPWM technique for ma=1

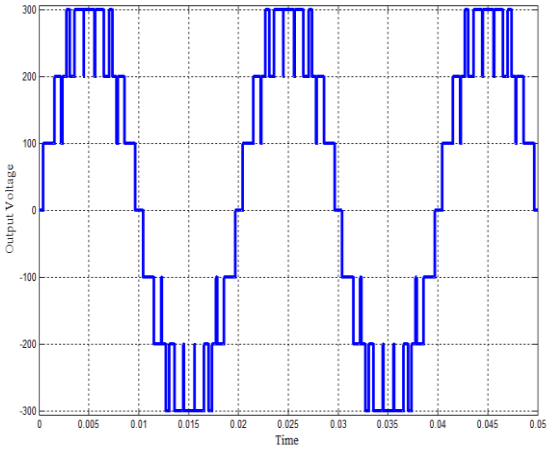

Fig.18 Output Voltage waveform of 7-Level Inverter

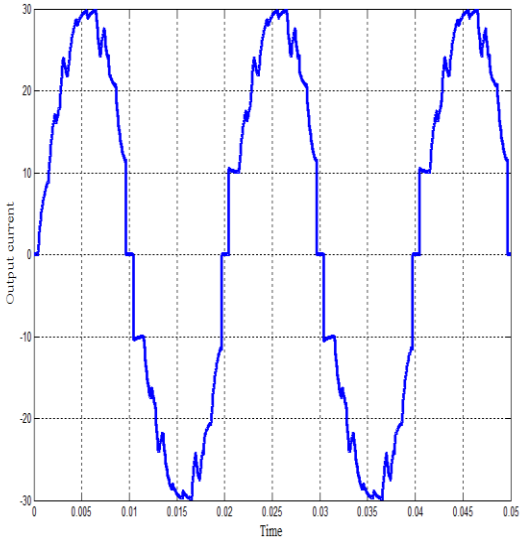

Fig.19 Output Current waveform(R-L Load) R=10 ohms L=5mH

Output voltage waveform for 7-level inverter is shown in Fig.18.Table II indicate THD values for various modulation techniques at different m_a values. Table III compares components used in various other conventional techniques with proposed topology and clearly indicates superiority of proposed topology over conventional inverters.

Table II Indicating %THD Values for various techniques at different modulation indices

Modulation technique	Modulation index(m_a)				
	1	0.95	0.9	0.85	0.8
PD	15.48	18.94	19.07	17.33	16.74
POD	14.57	16.67	18.61	20.45	22.26
APOD	17.15	18.89	20.51	22.19	22.21
ISCPWM	16.07	18.38	19.40	18.95	17.26

Table III Comparison between proposed topology and conventional topologies

Inverter topology	NPC	Flying capacitors	CHB	Proposed topology
Main switches	12	12	12	7
Main diodes	12	12	12	7
DC bus capacitors	6	6	3	3
Total components	30	30	27	17

VI.CONCLUSION

Conventional topologies uses more number of switching components hence switching losses increased rendering more power losses. Gate driver

requirement increases with more number of switches in conventional topologies hence cost is increased and efficiency is reduced. Third harmonic and low order harmonics must be nullified hence filter requirement increased but in proposed topology with less number of switches count 7-level output is produced and third harmonic is reduced. Hence losses has decreased so as cost and consequently efficiency increased.

VII.REFERENCES

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AshwiniOjhawas born in 17 march 1991 in Jhansi. He received his B.Tech degree from Babu Banarsidas National Institute of Technology and Management, Lucknow (U.P)in 2014 and currentlypursuing M.E. with specialization in Industrial systems and drives from Madhav Institute of Technology and Science (MITS, Gwalior) in Gwalior (2016-2018).

Praveen Bansalobtained his bachelor of Engineering (Hon's) in Electrical Engineering from Madhav Institute of Technology and Science(MITS),Gwalior in 2009,MTech degree in Electrical Drives from Maulana Azad National Institute of Technology in 2012,Currently he is an Assistant Professor at MITS, Gwalior. His area of interests includes multilevel Inverters, Induction motor modeling, and PWM techniques