Design and Implementation of 24/12 V DC-DC Buck Converter for 1 kW Wind Turbine

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***Abstract*— 1 kW Wind Turbine consists of 3 phase permanent magnet wind generator, 3 phase rectifier module with 24 V DC output, DC to DC converter with 12 V output, charge controlled section and inverter section to feed 220V/50 Hz to the load. In this paper, 24 to 12 V DC to DC buck converter for 1 kW wind turbine has been designed and implemented. Design calculation of components used is carried out according to design equations of buck converter. To achieve the regulated output of 12 V DC, DC-DC converter has been designed and simulated. Digital Pulse Width Modulator (DPWM) architecture using counter comparator architecture has been designed with switching frequency of 20 kHz in order to achieve the good conversion performance. Simulation results using Multisim software in order to verify the design requirements.**

***Index Terms*— Buck converter, components used, DPWM, counter-comparator, Multisim.**

INTRODUCTION

Design and construction of 1 kW wind turbine project has been undertaking as a combined research work of four engineering departments. Electronic engineering department has led as focal department of this project. Figure 1 shows the proposed block diagram of 1 kW wind turbine project. In this paper, the design of PID controlled buck converter is presented. Conventional design of PI Buck Converter has been modified by using PID compensator. Initially, simplified buck converter design was considered to meet design requirements, and then digital controlled converter design was introduced to enhance the front end design of the proposed system.

Digital control systems have significant advantages over conventional analog pulse width modulators (PWMs). In switching-mode converters, transistors are operated as switches, which inherently dissipate much less power than transistors operated as dependent current sources. Three basic configurations of switching regulators are step-down (Buck), step-up (Boost), and inverting (Buck-Boost). The basic idea for a step-down (Buck Converter) type is shown in the simplified circuit shown in the Figure 2.

The basic control element is a high-speed switch, which opens and closes rapidly from a control circuit that senses the output, and it adjusts the on-time and the off-time to keep the desired output. MOSFET transistors can switch faster than BJTs and have been improved in recent years, so they have become the preferred type of switching device, provided that the off-state voltage is not too high.

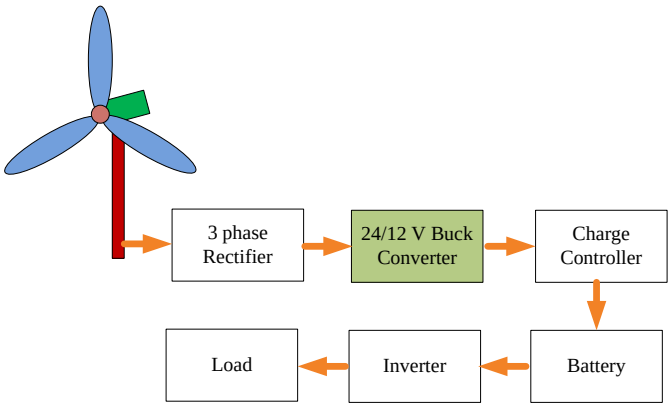

Figure 1. Block Diagram of proposed system

As in most electronic devices, there are trade-offs for designers in choosing a switching device. Differences in break-down voltage, on-state resistance, and switching time must all be considered for a given design. The pulsed current from the transistor switch is smoothed by an LC filter. The inductor tries to keep current constant, and the capacitor tends to keep voltage constant. Ideally, these components do not dissipate power, but in practice some loss is encountered due to various factors.

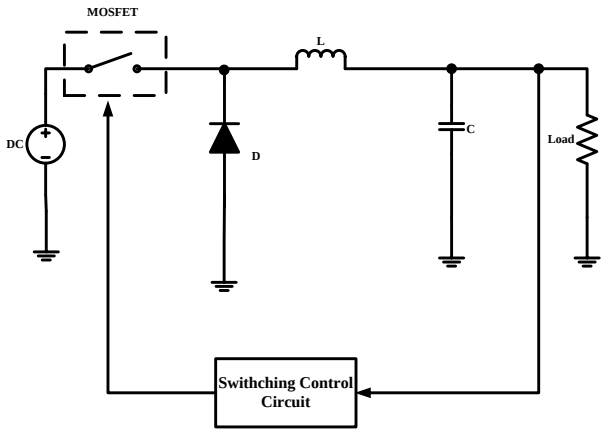

Figure 2. Simplified Buck Converter

To avoid requiring large (and expensive) inductors and capacitors, the switching frequency is selected to be much higher than the utility frequency; 20 kHz is common. The switching frequency usually ranges from 25 to 500 kHz. To avoid audio noise, the switching frequency should be above

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20 kHz. A PWM switching-mode voltage regulator generates a high-frequency rectangular voltage wave, which is rectified and filtered.

The duty cycle (or the pulse width) of the rectangular wave is varied to control the dc output voltage. Therefore, these voltage regulators are called PWM dc–dc converters. Power converters are required to convert one form of electric energy to another. A dc–dc converter is a power supply that converts a dc input voltage into a desired regulated dc output voltage. PWM regulators are used at high power.

They are small in size, light in weight, and have high conversion efficiency. The on and off intervals of MOSFET Q1 are shown in the waveform of Figure 3 (a). For an n-channel D-MOSFET, the control voltage swings between a negative value (off) to a positive value (on). The capacitor charges during the on-time (t_{on}) and discharges during the off-time (t_{off}) [2].

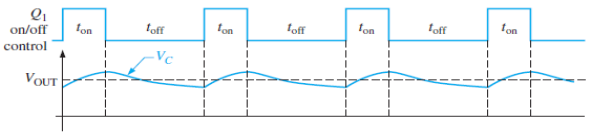

Figure 3 (a). V_{OUT} depends on the duty cycle [2]

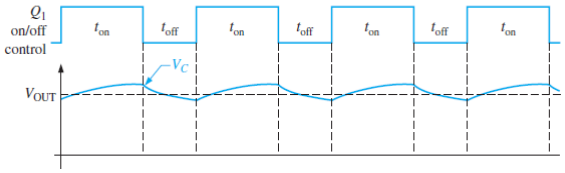

Figure 3 (b). Increase the duty cycle and V_{OUT} increases [2]

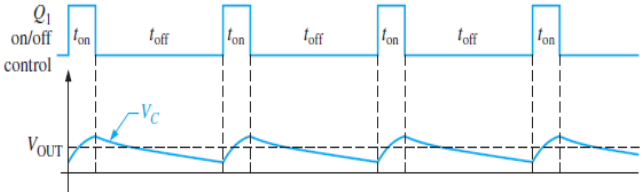

Figure 3 (c). Decrease the duty cycle and V_{OUT} decreases [2]

When the on-time is increased relative to the off-time, the capacitor charges more, then increasing the output voltage, as indicated in Figure 3 (b). When the on-time is decreased relative to the off-time, the capacitor discharges more, thus decreasing the output voltage, as in Figure 3 (c). The inductor further smoothes the fluctuations of the output voltage caused by the charging and discharging action.

The regulating action is as follows: When V_{OUT} tries to decrease, the on-time of Q_1 is increased, causing an additional charge on *C to offset the* attempted decrease. When V_{OUT} tries to increase, the on-time of Q_1 is decreased, causing the capacitor to discharge enough to offset the attempted increase [2].

2) Digital Controlled DC-DC Buck Converter

Fig. 4 shows the circuit diagram of digital controlled DC–DC buck converter. In the digitally controlled loop, the output of Analog to Digital Converter (ADC) is compared to the desired reference value, V_{REF}, the resulting error signal, is minimized through the action of the PID compensator which generates a din, trying to maintain approximately low error signal and develop the dynamic performance of the whole system.

The compensator output gives digital representation of the duty cycle, represented in discrete format from the Most Significant Bit (MSB) to Least Significant Bit (LSB). The output of compensator is followed by the DPWM which translates the discrete duty cycle command and controlling the ON–time of the main power MOSFET. Consequently, a well designed PID compensator and high resolution DPWM architecture are essential to achieve a firmly regulated converter output.

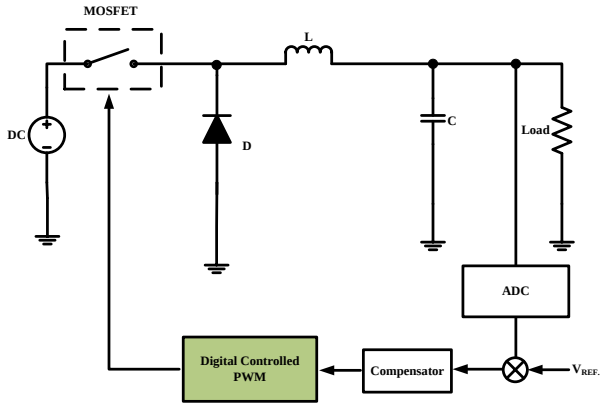

Figure 4. Digitally Controlled DC–DC Buck Converter

In this research, the calculations of the values of inductor, capacitor, high speed high frequency diode and MOSFET selection are carried out. DPWM architecture using counter comparator architecture has been designed as well. DPWM resolution is proportional to the switching frequency.

The resolution of the DPWM is very important in deciding the accuracy and the overall performance of the converter. The higher the resolution, the higher the sampling frequency required which can be impractical and costly. Some designers sample at frequencies around ten times higher than the switching frequencies to minimize the phase delay.

PWM Architecture

The functional block diagram of the counter comparator architecture is shown in Fig. 5. The system input is an n-bit data word, corresponding to the desired PWM duty cycle. The register output loaded the n-bit data input, is compared with the output of synchronous counter.

When these two values become equal, the comparator output is used to reset the S/R latch output which produces the PWM signal. The S/R latch output is set when the counter reaches an overflow condition at the end of a PWM period. At the same time, the overflow signal is used to load the n-bit data input to the input register, so that the duty cycle of PWM output is updated the new PWM signal.

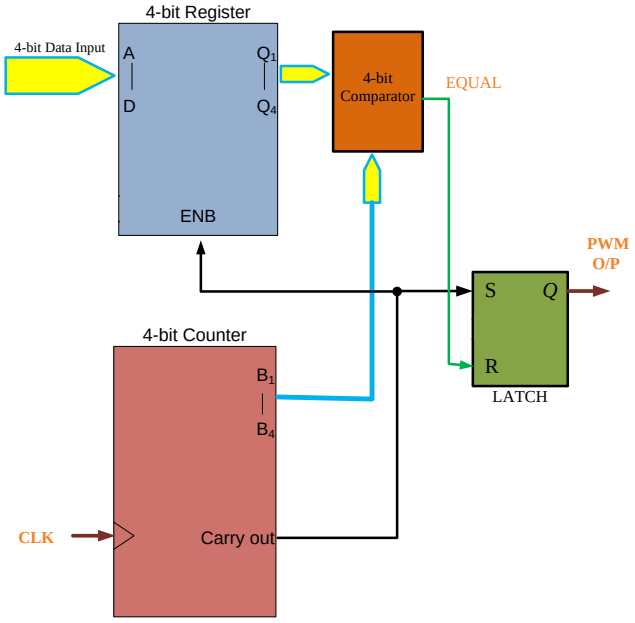

Figure 5. Block Diagram of the counter comparator PWM Architecture

3) Design Considerations

The DC output voltage is regulated to the desired value by adjusting the reference voltage value, thus modifying the PWM signal duty cycle [5], as follows:

$$V_o = D.V_{in} = (T_{on}/ T_s). V_{in} \qquad Eq.(1)$$

where Vin is the converter DC input voltage, 'D' is duty cycle of the PWM signal ($0 \leq D \leq 1$), 't_{on}' is 'ON' time of the PWM signal and T_s is the converter switching period.

The PWM frequency is calculated by using Eq. (2), while its duty cycle is given from the equation:

$$D = (Data\ \_Value)/ 2^N \qquad Eq.(2)$$

where Data_Value is the input data word integer value If an 4-bit input is used, then the duty cycle is in the range $0 \leq D \leq (15/16)=93.75\%$.

Since the PWM duty cycle has 2^N different states, the generator resolution, α, is defined as

$$\alpha=(1/ 2^N).100\% \qquad Eq.(3)$$

In order to achieve high PWM frequencies, resulting in high clock rates, a fast counter is required.

Design of Components Used in Buck Converter

The duty cycle can be calculated using the equation (1), thus D = 0.5. The calculation of inductor is determined using the following equation [1]:

$$L_{min} = ((1-D) .R)/(2f_s) \qquad Eq.(4)$$

where, R is the load resistance used and f_s is switching frequency used.

The calculation of capacitor is determined using the following equation [1]:

$$C = (1-D) /8L\ V_r\ (f_s)^2 \qquad Eq.(5)$$

where, L is the inductance used and V_r is output voltage ripple factor used.

4) Simulation Results

Firstly, simulation with Multisim 12 software has been done for 24 V to 12 V Buck converter using 50 % duty cycle. Simulation has shown in Figure 6. Then, Simulation has done for (4-bit) counter-comparator architecture used in PWM design. Circuit Diagram used to simulate with Multisim is shown in Figure 7. Figure 8 and 9 are the results of data input '1000' and '0001'. PWM output has been verified using counter-comparator architecture. The duty cycle is in the range $0 \leq D \leq (15/16) = 93.75\%$. PWM duty cycle has 2N different states, the generator resolution, α, is 6.25.

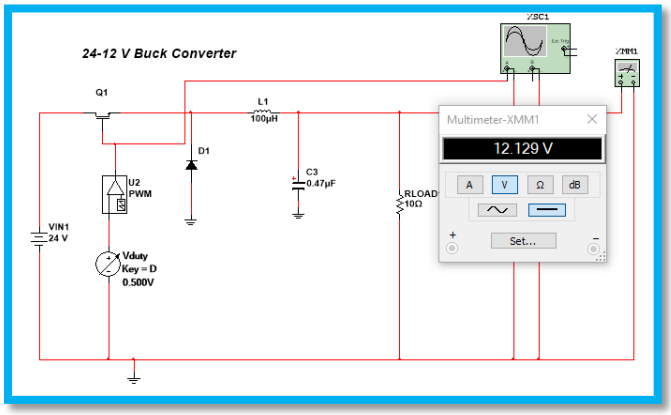

Figure 6. Simulation of Buck Converter

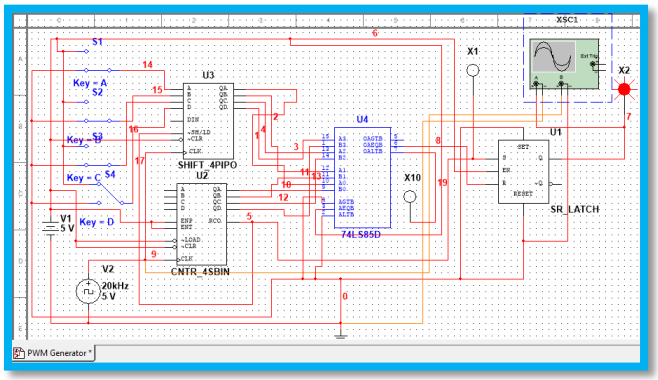

Figure 7. Multisim simulation of counter-comparator (4-bit)

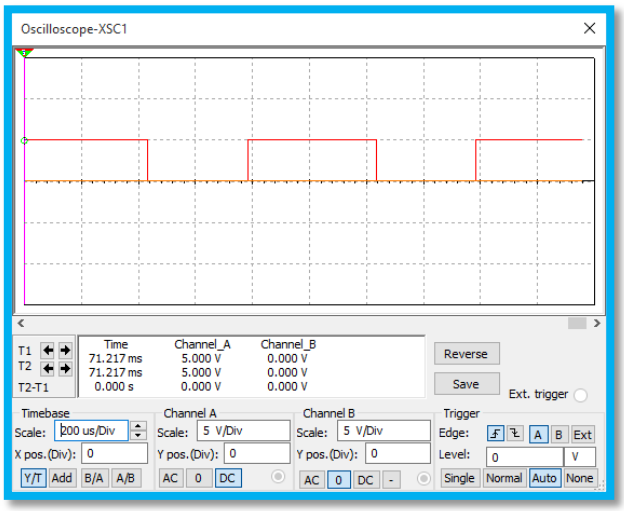

Figure 8. Multisim simulation of counter-comparator (data input '1000')

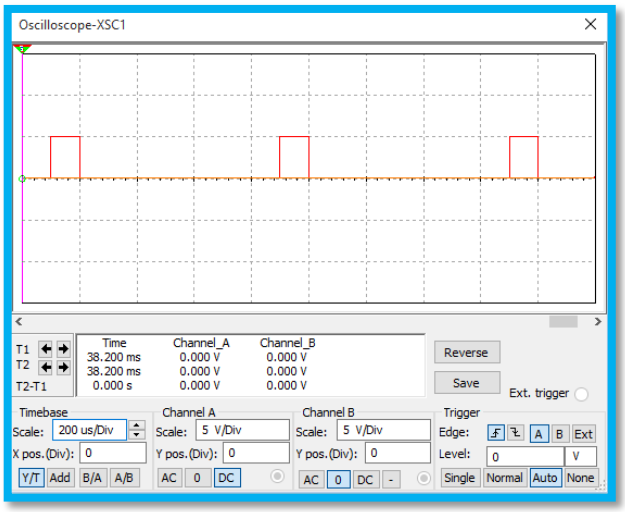

Figure 9. Multisim simulation of counter-comparator (data input '0001')

Parallel data come to data input of the register has been loaded simultaneously and parallel loaded data will be compared with output of the synchronous counter, consequently the output signal will be generated to perform the reset output of the PWM signal. The simulation result of SR latch output has been verified. In order to avoid the limit cycle constraint, if DPWM resolution is used for n-bit because the selected ADC is of (n-1)-bit resolution.

5) CONCLUSION

The calculations for the L, C values are verified using Multisim 12 Software to get required DC output voltage. Digital pulse width modulator has been designed using 4 bit counter-comparator architecture; the duty cycle is in the range $0 \leq D \leq 93.75\%$. PWM duty cycle has 2^N different states, the generator resolution, α, is 6.25. The desired switching frequency of 20 kHz and clock frequency have to be used by function generator to test the initial design. The final design will be tested by constructing the local oscillator or by using suitable integrated circuit. To avoid the limit cycle constraint, if DPWM resolution is used for n-bit, the selected ADC is of (n-1)-bit resolution.

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REFERENCES

[1] Ali Emadi, Alireza Khaligh, Zhong Nie, Young-Joo Lee, J. F., *Integrated Power Electronic Converters and Digital Control. CRC Press Taylor & Francis Group. Boca Raton, FL* 33487–2742, (2009).

[2] Thomas L. Floyd, *Digital Fundamentals, 9th Edition, Pearson International Edition*, ISBN-0-13: 197255-3, Prentice Hall, (2006).

[3] MARIAN K. KAZIMIERCZUK, Wright State University, Dayton, Ohio, *Pulse-width Modulated DC–DC Power Converters, 1st Edition, A John Wiley and Sons, Ltd, Publication*, ISBN-978-0-470-77301-7, John Wiley & Sons, Ltd, USA (2008).

[4] Peter J. Ashenden, *Digital Design – An Embedded Systems Approach using VERILOG*. ISBN 978-0-12-369527-7, United States, (2008).

[5] S.C. Huerta, A. de Castro, O. Garcia, J.A Cobos, *"FPGA Based Digital Pulse Width Modulator with Time Resolution under 2 ns," IEEE Trans. on Power Electronics, vol. 23, no. 6, pp. 3135–3141*, November 2008.

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