Double Tail Dynamic Comparator using 180nm Technology

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Abstract— **The exigency for ultra-low-power, high speed and space economical analog-to-digital converters are driving toward the employment of dynamic regenerative comparators to maximise speed and power potency. This paper describes the Double Tail Dynamic Comparator designed in 180nm CMOS Technology. The circuit works on very less power supply of 700mV. The power dissipation of the circuit is approx. 8.01 µW. Slew rate of the circuit is quite high. The design work at the 100MHz of frequency it is shown that in the proposed dynamic comparator both the power consumption and delay time are significantly reduced.**

Index Terms— **Dynamic clocked comparator, Double-tail comparator, high-speed analog-to- digital converters (ADCs), low-power analog design, Adaptive biasing differential pair**

1) INTRODUCTION

Conventionally, comparators are circuit elements, that compare's two analog input voltages and give output as a logical value, which depends on the duality of the input voltage difference. Hence such circuits are needed for the conversion from the analog domain into the digital domain [1]. COMPARATOR is used as one of the fundamental building blocks for most of the analog-to-digital converters (ADCs). ADCs, such as flash ADCs, Sigma-delta ADC require low-power and high-speed comparators with small chip area. When considering the fact that threshold voltages of the devices have not been scaled at the same pace as the supply voltages of the modern CMOS processes in high-speed comparators at ultra-deep sub micrometer (UDSM) CMOS technologies suffer from low supply voltages [2]. Therefore, designing high-speed comparators is more difficult when the supply voltage is smaller. In different words, in an exceedingly given technology, to attain high speed, larger transistors are needed to compensate the reduction of provide voltage, that additionally means a lot of die space and power is required To overcome the limitation in slew rate at the constant input biasing linear amplifier, an adaptive biasing scheme with AB class input stage operation is implemented by the flipped voltage follower (FVF). Section II describes the proposed dynamic double tail comparator .Section III presents detailed circuit design for the proposed dynamic double tail comparator. Section IV presents experimental results. Conclusions are provided in Section V.

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2. PROPOSED DYNAMIC DOUBLE TAIL COMPARATOR

A. Flipped voltage follower (FVF) structure

Fig.1 (a) presents a basic flipped voltage follower (FVF) structure. Comparing to the PMOS version conventional voltage follower, it moves the current biasing from the to the bottom of the transistor *M*1 and a shunt feedback is added around it. This FVF can source more current to load but sinking capability is limited by the biasing current *IB*. The open loop small signal analysis has been elaborated in [3]

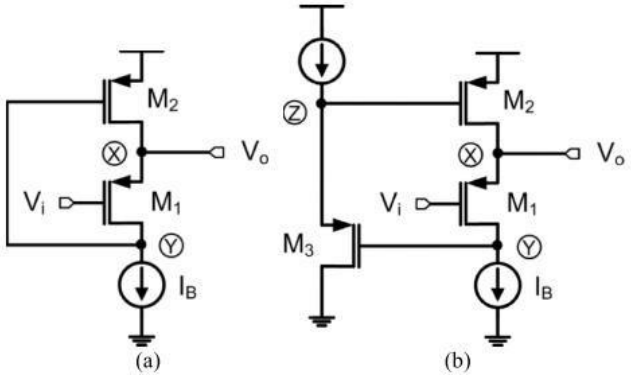


Fig.1 (a) Basic FVF structure from (b) High supply version FVF structure after

Fig.1 By breaking the loop at node *Y* we can obtain the open loop gain and the value is given by equation (1). *rolY*, shown in (2), is the open loop small signal impedance at node *Y*. Two poles in the loop are located at node *X* and *Y*, respectively, *rolX* is a low impedance node compared to node *Y*. Since the dominant pole is located at node Y, $\omega Y <$ UGF $< \omega X$, in some cases compensation is required at node Y to ensure flipped voltage follower loop stability [3],[4]

$$Av_{01} = -gm_2 r_{01} Y \qquad (1)$$

$$r_{01}Y = r_B \| gm_1 r_{01} r_{02} \approx r_B \qquad (2)$$

Flipped voltage follower is suitable for low voltage operation, since the minimum operating supply voltage for this amplifier *is* $VDD_{min}=V_{sg} + Vd_{sat}$, and in advanced technology nodes, VDD_{min} can be lower than 1 V. Hence, if supply voltage is close to 3.3 V, the common mode range of *Vi* would be limited by V_{sg2}. the size of transistor *M*2 should be small to overcome this limitation. Fig.1 (b) shows a high supply voltage version FVF. By adding a voltage follower *M*3, V_i can achieve even larger common mode range from $VDD - 3V_{sg} + Vd_{sat}$ *to* $VDD - V_{sg} - Vd_{sat}$. Whereas, node Z is an additional pole added to the loop that should be pushed out for stability

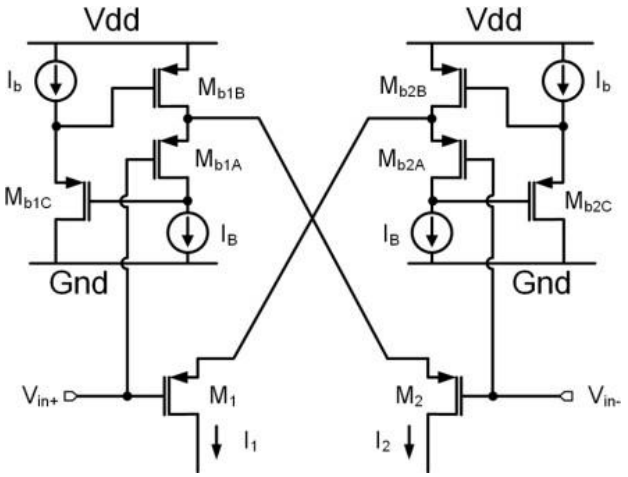


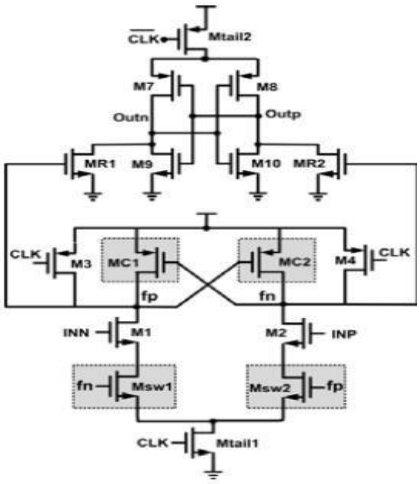
Fig.2 Adaptive biasing differential pair

B. Double tail regenerative comparators

Most of the ADC's today use double tail regenerative comparator as the building blocks for high-speed and they can make fast decisions due to the strong positive feedback in the regenerative latch. Latterly, many analyses have been presented, which investigate the performance of these comparators from different feature, such as noise [5], offset [6], [7], and [8], and kick-back noise [9], random decision errors [10].

A dynamic double-tail comparator is shown in Fig. 3 [11]. This topography has less stacking and therefore can operate at lower supply voltages compared to the conventional dynamic comparator. The double tail enables both a large current in the latching stage and wider M_{tail2},

for fast latching independent of the input common-mode voltage (V_{cm}), and a small current in the input stage (small



M_{tail1}), for low offset [12].

Fig.3 Double tail regenerative comparator

3. CIRCUIT DESIGN

Fig. 4 demonstrates the schematic diagram of the proposed dynamic double-tail comparator. The proposed comparator is designed based on the double-tail structure, due to the better performance of double-tail architecture in low-voltage applications. The main idea of the proposed comparator is to increase *Vfn/fp* in order to increase the latch regeneration speed.

Operation of the Proposed Comparator

The operation of the proposed comparator is as follows (see Fig. 4). During reset phase (*CLK = 0*, M_{tail1} and M_{tail2} are *OFF*, avoiding static power), transistor *M5* and *M6* pulls both *fn* and *fp* nodes to *VDD*, hence transistor *M8* and *M7* are cut *OFF*. Transitional stage transistors, *M9* and *M11*, reset both latch outputs to ground.

During decision-making phase (*CLK = VDD*, M_{tail1}, and M_{tail2} are *ON*), transistors *M5* and *M6* turn *OFF*. Hence, at the beginning of this phase, the control transistors are still off (since *fn* and *fp* are about *VDD*). Thus, *fn* and *fp* start to drop with different rates according to the provided input voltages. Suppose *VINP*

> *VINN*, thus node *fp* drops faster than node *fn*, (since *M2* provides more current than *M4*). As long as node *fp* continues falling, the corresponding PMOS control transistor i.e. *M7* starts to turn *ON*, pulling *fn* node back to the *VDD*, so another control transistor (*M8*) remains *OFF*, allowing node *fp* to be discharged completely.

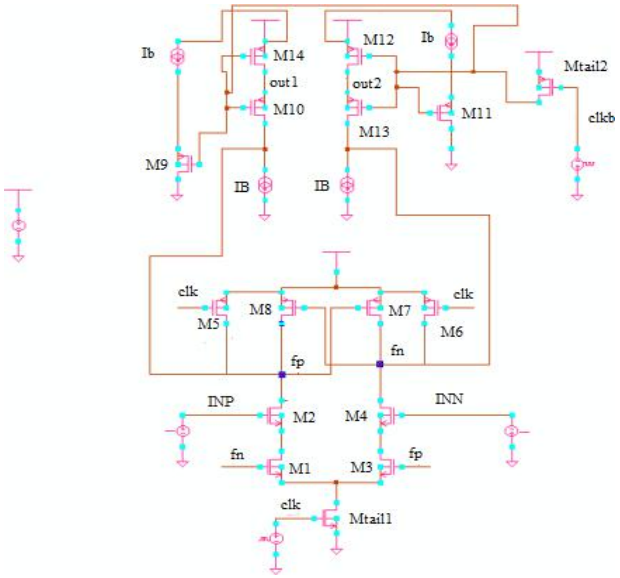


Fig. 4 Proposed dynamic double tail comparator

4. SIMULATION RESULTS

The circuit has been simulated at 0.18 µm CMOS Technology. Circuit operates on the supply voltage of 700mV. The experimental results are presented in the table.

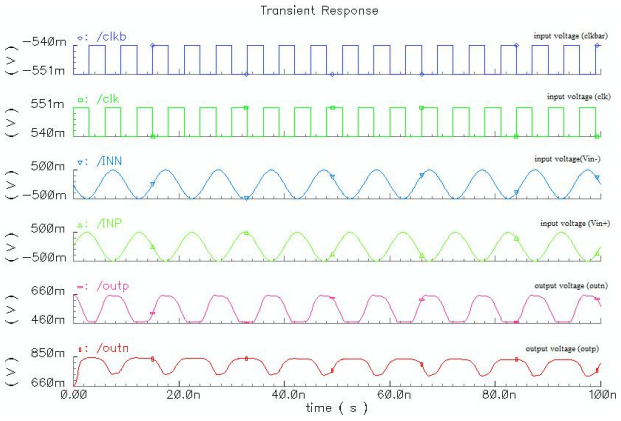


Fig.5 Transient analysis of proposed Comparator

Table i: result of proposed comparator

Design parameters	**Comparator Value**
Technology	180nm
Supply voltage	700 mV
Slew rate+	79.0997 M
Slew rate-	70.1998 M
Rise time	0.1 ns
Fall time	0.6 ns
Hold time	0.6 ns
Delay	0.01 ns
Power dissipation	8.119 µw

5. CONCLUSION

In this paper a new dynamic double tail comparator with low-voltage low-power capability was proposed in order to improve the performance of the comparator. The proposed circuit is simulated in 0.18µm CMOS Technology. The delay of the proposed circuit is reduced; power dissipation of the circuit is very less as compare to the conventional dynamic double tail comparator. And the speed of the circuit is maximized as the slew rate of the circuit is quite high.

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